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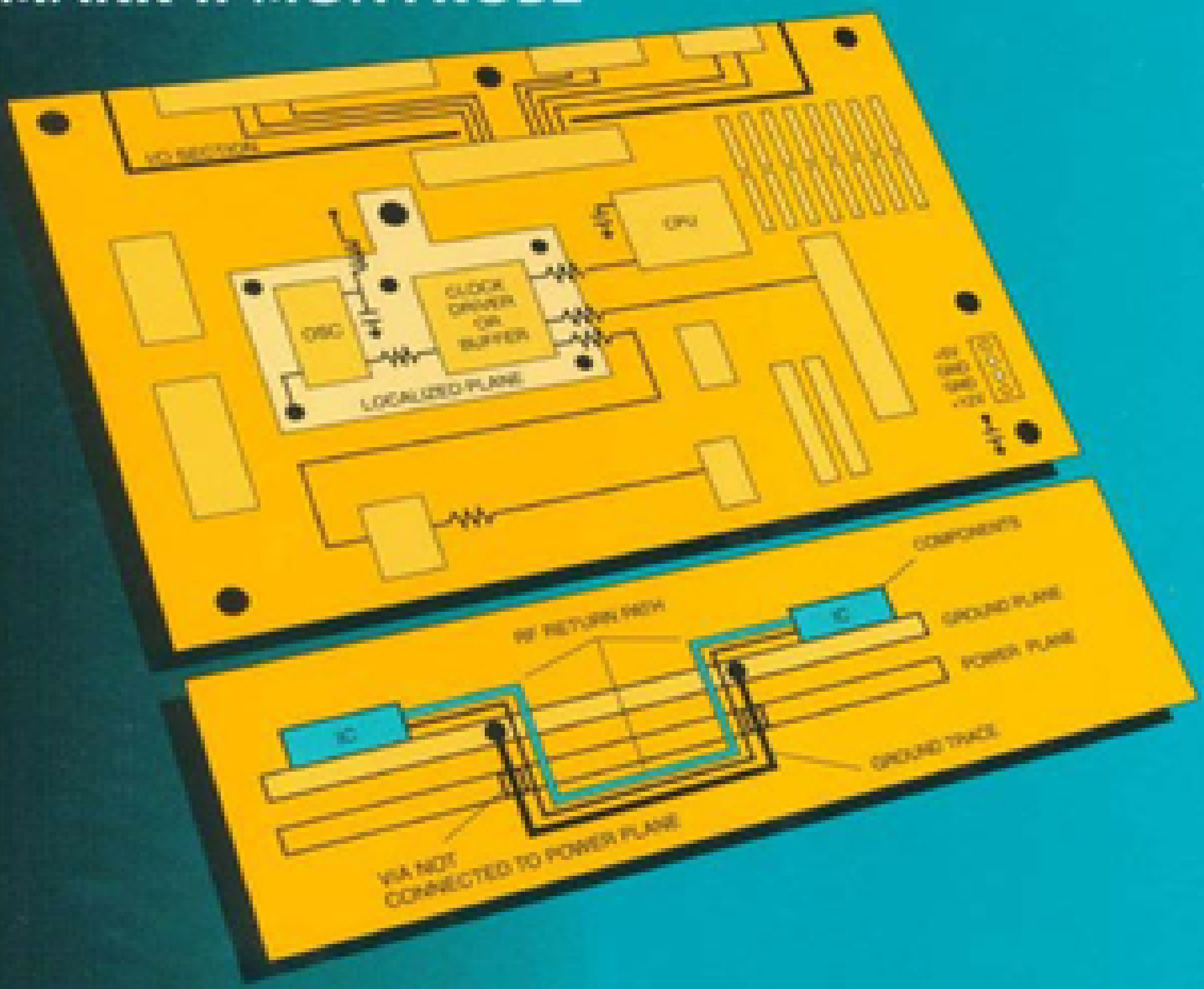
PRINTED CIRCUIT BOARD DESIGN TECHNIQUES FOR EMC COMPLIANCE

SECOND EDITION

A Handbook for Designers

MARK I. MONTROSE



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by Mark I. Montrose

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Recommend this title? yes no

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Mark I. Montrose

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To my Family

Margaret, Maralena, and Matthew

Acknowledgments

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My appreciation and acknowledgment to Elya B. Joffe of K.T.M. Project Engineering, Ltd., Israel, for extended discussions related to EMC and PCB theory. His technical review for accuracy was extensive and comprehensive.

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My very special acknowledgment is to my wife Margaret and my two children Maralena and Matthew. Again, my family tolerated my efforts to rewrite this book, after writing two previous books over the course of many years. They supported me working during the day as a consultant, while doing my writing at night and on weekends. They also supported me during extended travels around the world teaching, consulting, and keeping abreast of new technology related to printed circuit boards, which meant many long hours away from home.

Mark I. Montrose
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About the Author

Mark I. Montrose graduated from California Polytechnic State University, San Luis Obispo, CA, with a B.S. degree in electrical engineering and a B.S. degree in computer science in 1979. In 1983 he received a master of science-engineering management degree from the University of Santa Clara, CA.

Mr. Montrose has many years of experience in the field of regulatory compliance, electromagnetic compatibility, and product safety. His experience includes extensive design, test, and certification of information technology equipment. He specializes in the international arena, including the European EMC, machinery, and low-voltage directives for light industrial, residential, and heavy industrial equipment.

An active participant in local, national, and international activities of the IEEE (Institute of Electrical and Electronics Engineers) and the EMC Society, Mr. Montrose is a member of the Board of Directors of the IEEE EMC Society. He is a senior member of the IEEE and a life member of the American Radio Relay League (ARRL) with the Amateur Extra Class License, K6WJ. In addition, he is a distinguished lecturer for the IEEE EMC Society, a director of TC-8 (Product Safety Technical Committee of the IEEE EMC Society), and a member of the dB Society, as well as a member of the Editorial Review Board for several EMC publications.

In 1999 Mr. Montrose authored another best-selling reference textbook, *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple*, also published by IEEE Press. He has authored and presented numerous technical papers in the field of EMC and signal integrity for high-technology products, printed circuit board (PCB) design, and EMC theory at international EMC symposiums and colloquiums in North America, Europe, and Asia. Mr. Montrose is certified by California's Council for Private Postsecondary and Vocational Education in PCB technology. He provides accredited PCB design and layout seminars to corporate clients worldwide.

Mark I. Montrose is an expert in the fields of regulatory compliance, electromagnetic compatibility and product safety including extensive research, design, test and certification for various product categories. He has authored and presented a myriad of papers on the topics of EMC theory and signal integrity at both commercial and EMC symposiums and colloquiums throughout North America, Europe, and Asia.

Mr. Montrose is a senior member of the IEEE (Institute of Electrical and Electronics Engineers) and a member of the Board of Directors of the IEEE EMC Society. In addition, he is a distinguished lecturer for the society and active participant in local, national, and international activities of the society. Moreover, Mr. Montrose is the author of the best-selling companion book, *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple* (IEEE Press, 1999). This engineering-level book explains how and why all concepts within *Printed Circuit Board Design Techniques for EMC Compliance* work.

Preface

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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Recommend this title? yes no

Preface

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition, is a significant enhancement to the first edition. The first edition was well received within the engineering community worldwide and was translated into international languages. The intent of the present volume is to expand upon concepts presented in the earlier edition, to justify why a specific design technique works, and to show when it is appropriate for use. Additional techniques based on technological changes within the last few years are also incorporated. These techniques and enhancements are based on questions, comments, and discussions received from engineers around the world.

This book presents information never before published within the engineering community, dealing exclusively with printed circuit boards (PCBs). When writing the first edition, it was impossible to anticipate the amount of variations possible, or what the intended audience expected from a book directed toward nondegreed engineers. A thorough understanding of the concepts presented herein will assist during the design and layout process. Note the key word here —"concepts."

Printed Circuit Board Design Techniques for EMC Compliance will help minimize the emission or reception of unwanted radio frequency (RF) energy generated by components and circuits, thus achieving acceptable levels of electromagnetic compatibility (EMC) for electrical equipment. The field of EMC consists of two distinct areas:

1. Emissions: Propagation of electromagnetic interference (EMI) from noncompliant devices (culprits) and, in particular, radiated and conducted electromagnetic interference.

2. Susceptibility or immunity: The detrimental effects on susceptible devices (victims) in forms that include EMI, electrostatic discharge (ESD), and electrical overstress (EOS).

The primary goal of the engineer is to ensure proper operation and performance of a product when used within an intended electromagnetic environment. These design requirements are in addition to making a product function as desired for use within a specific, end-use environment.

Information presented in this guideline is intended for those who design and layout printed circuit boards. EMC and compliance engineers will also find the information presented herein helpful in solving design problems at both the PCB and system level. This book can be used as a reference document for any design project.

The focus of this book is *strictly* on the PCB. Containment techniques (shielding), internal and external cabling, power supply design, and other system-level subassemblies that use PCBs as a subcomponent will not be discussed. Again, as in the first edition, excellent reference material on these aspects of EMC system-level engineering is listed in the References section at the ends of chapters.

Circuit technology is advancing at a rapid rate. Design techniques that worked several years ago are no longer effective in today's products with high-speed digital circuits. As such, there is a need for introductory material that presents fundamental concepts in an easy to understand format. With this in mind, *Printed Circuit Board Design Techniques for EMC Compliance*

was written for engineers who never studied applied electromagnetics in school, or who have limited hands-on experience with high-speed, high-technology PCBs related to EMC compliance.

While it is impossible to anticipate every application or design concern possible, this book provides details on how to implement a variety of design techniques for most products, application dependent. The concepts presented are *fundamental* in nature. Although every design is different, the fundamentals of product design rarely change because electromagnetic theory is always constant. If fundamental concepts of EMC suppression at the PCB level are learned, implementation becomes a simple issue of practice, though every product will be different from previous designs.

This book presents a minimal amount of mathematical analysis and instead concentrates on *hands-on techniques* that have been successfully applied to many real-world products. Information is presented in a format that is easy to understand and implement. Those interested in Maxwell's equations, or in the more highly technical aspects of circuit theory related to PCB design should consult my companion book, *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple* (IEEE Press, 1999). The Reference sections and the bibliography also provide listings of publications that discuss EMC theory using rigorous mathematical analysis. These references are provided because a discussion of technical material is beyond the scope of this book.

The companion book, *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple* explains in engineering terms how and why EMC exists. The target audience for this edition is degreed engineers.

The main differences between my first and second books are as follows:

- *Printed Circuit Board Design Techniques for EMC Compliance*. Provides information for those who have to get a product designed and shipped within a reasonable time frame and within budget. It illustrates that a PCB may exhibit an EMI problem, it briefly explains why the problem occurs, and it shows how to solve the design flaw during layout. For the PCB designer, a show-me-how-to-do-it approach exists, with minimal mathematical analysis.

- *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple*. This is a companion book for designers who want to know how and why EMI is developed within a PCB. Although these designers may not be directly accountable for the actual PCB layout, they may be responsible for the end product. Engineers generally want to understand technical concepts. This book elucidates a subject that is generally not taught in universities or other educational environments, again using a minimal amount of math.

Controlling emissions has become a necessity in designing electronic devices for both the civilian and military environment. It is more cost-effective to design a product with suppression designed into the PCB than to "build a better box." Containment measures are not always economically justified and may degrade as the EMC life cycle of the product is extended beyond the original design specification. For example, users usually remove covers from enclosures for ease of access during repair or upgrade. In many cases, sheet metal covers, particularly internal subassembly covers that act as partition shields are never replaced. The same is true for blank metal panels or faceplates on the front or rear of a system that contains a chasis or backplane assembly. Consequently, containment measures are compromised, and electromagnetic compatibility with the end-use environment is affected. Proper layout of a PCB, with suppression techniques implemented, assists EMC compliance at the level of cables and interconnects, whereas box shielding (containment) does not.

Why worry about EMC compliance? After all, isn't speed the most important design parameter as mandated by a marketing specification? Internationally, legal requirements dictate the maximum permissible interference potential of digital products. These requirements are based on experience in the marketplace and are related to emission and immunity complaints. Often, these same techniques will help improve signal quality and signal-to-noise ratio performance.

This text discusses both high- and low-speed designs that require new and expanded layout techniques for EMC suppression at the PCB level. Most techniques used several years ago are now less effective for proper signal functionality and compliance. Components have become faster and more complex. Use of custom gate array logic, application-specific integrated circuits (ASICs), ball grid arrays (BGAs), multichip modules (MCMs), flip chip technology, and other digital devices operating in the sub-nanosecond range present new and challenging opportunities for EMC engineers. Technology is progressing at an incredible rate. It is becoming impossible for an engineer to keep up with the technical details and aspects of various logic devices available for use. Even if an engineer learns everything about a new type of logic family, implementation of these devices on the PCB may be overshadowed by other concerns. These concerns include Input/Output (I/O) interconnects, mixed logic families, different voltage levels, analog and digital components, and packaging requirements. The design and layout of a PCB for EMI suppression at the source must always be optimized, while maintaining systemwide functionality. This is a job for both the electrical design engineer and the PCB designer.

In order to design and create a PCB, use of simulation software is becoming mandatory during the development cycle. Simulation software will not be discussed herein, because the requirements for performance, features, and integration between platforms and vendors frequently change. Where appropriate, simulation tools will be mentioned.

In an effort to keep costs down, design for manufacturing (DFM) concerns must also be addressed. In addition, test points must be provided for all nets. For very sophisticated PCBs, DFM and test points may have to give way to functional requirements. If the PCB designer is not knowledgeable or aware of other facets of PCB layout during the design stage, besides placing components and routing traces, serious functionality concerns will develop. In addition, the PCB will usually fail signal integrity and EMC tests, requiring a forced relayout of the board.

Significant changes have been made in the second edition of this book, including:

- Restructuring of chapters by moving material elsewhere for a better flow of information, placing related topics together instead of being scattered throughout the book.
- Addition of subject headers to various sections within the text for ease of identification of the topic being discussed. In various places, two items that were blended together in the first edition are now separated to facilitate understanding.
- Inclusion of new and advanced layout techniques based on technology and knowledge that became available after the release of the first edition.
- Major overhaul of Chapter 2 (Printed Circuit Board Basics) and Chapter 3 (Bypassing and Decoupling). These are two of the more important chapters in this book. An expansion on the fundamentals of PCB design is presented for engineers who want a thorough understanding, in simplified form, of why layout techniques work the way they do. Because engineers generally want to understand how and why things work, a primer on PCB theory is now incorporated. New concepts related to bypassing and decoupling techniques mandated a complete restructuring of Chapter 3.
- Clarification on when a particular technique is appropriate and not appropriate for use. Justification on how various techniques work is now provided.
- Greatly enhanced information related to single- and double-sided stackup assemblies.
- Restructuring and extensive enhancement of Chapter 4, focusing on all aspects of transmission line (traces) within the PCB in one complete chapter, without having to jump to different areas for a sequential flow of information.
- Clarification and expansion on I/O and interconnects (Chapter 5).

- Significant embellishment of Chapter 6, with sections on additional prevention, layout, and control techniques.
- Restructuring of Chapter 7, including new chapter headings to describe contents as appropriate. Material presented in the first edition was grouped together under one subheading, and new layout techniques were added.
- Chapter 8 is significantly different, as unique layout techniques are now grouped into one chapter. Also, technical details on right angle corners and the 20-H rule are presented. This information has *never* been published in any written form world-wide, until now.

Information in this edition will assist in PCB design and layout, with the intent of meeting North American and international EMC compliance requirements. Many different layout design methodologies exist. This book illustrates generally applicable layout methods for EMC compliance, along with a justification of why the technique works. The concepts presented will vary for each particular PCB design.

Engineers may focus on analog, digital, or system-level products but, regardless of specialty, whatever they produce must be suitable for production. Frequently, more emphasis is placed on functionality than on system integration, with system integration usually assigned to product engineers, mechanical engineers, or others within an organization. Design engineers must now consider other aspects of product design, including the layout and production of PCBs for EMC compliance. Considerations include recognition of the way the electromagnetic fields transfer from circuit boards to the chassis and/or case structure. In addition, cost must be minimized during design, test, integration, and production.

If a product fails to meet regulatory compliance tests (EMC and product safety), redesign or rework may be required. This redesign significantly increases costs such as the following:

1. Engineering resources (along with administrative overhead).
2. A new PCB layout, including artwork and gerber files.
3. Prototyping material required for a new product build.
4. System integration and testing to validate functionality and compliance.
5. Procurement of new or additional components for quick delivery (very expensive).
6. New or modified in-circuit test fixtures and documentation.
7. Retesting for EMC compliance and product safety.

These costs are in addition to loss of market share, delayed shipments, loss of customer faith in the company (goodwill), a potential drop in stock price, anxiety attacks, as well as many other issues not detailed in the list. Personal experience as a consultant has allowed me the opportunity to witness several times such problems faced by start-up companies.

Not only must a design work properly, it must also comply with international regulatory requirements. Engineers who specialize in regulatory issues must evaluate products based on different standards. The present guide describes techniques that will alleviate existing conflicts among various layout methods.

A great deal of technical information related to PCB design and layout is available commercially, as well as from public domain documents. Typically, these sources provide only a brief discussion of how to implement a layout technique to solve an EMI problem without justifying the need, use, or application. (Several sources are listed in the Bibliography.)

My focus as a consultant is to assist and advise in the design of high-technology products at minimal cost. Implementing suppression techniques saves money, enhances performance, increases reliability, and achieves first-time compliance with emissions and immunity requirements, in

addition to having the product function as desired.

This industry has allowed me to participate in state-of-the-art designs as we move into the future. Although my focus is on the technology of the future, one cannot forget that simple, low-technology products are being produced in ever increasing numbers. Although the thrust of this book is toward high-end products, an understanding of the fundamental concept of EMC suppression techniques will allow any PCB being designed to pass EMC tests. When one does not understand fundamental concepts, compliance and functional disaster may be the result.

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Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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A guide for engineers who want to reduce unwanted electromagnetic fields and radio frequency interference on their circuit boards.

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Chapter 1 - Introduction

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Chapter 1: Introduction

1.1 FUNDAMENTAL DEFINITIONS

The following basic terms are used throughout this book.

Containment. A process whereby RF energy is prevented from exiting an enclosure, generally by shielding a product within a metal enclosure (Faraday cage or Gaussian structure) or by using a plastic housing with an RF conductive coating. Reciprocally, we can also speak of containment as preventing RF energy from entering the enclosure.

Electromagnetic compatibility (EMC). The capability of electrical and electronic systems, equipment, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels or performance, without suffering or causing unacceptable degradation as a result of electromagnetic interference (ANSI C64.14-1992).

> *Electromagnetic interference (EMI)*. The lack of EMC, since the essence of interference is the lack of compatibility. EMI is the process by which disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths (or both). In common usage, the term refers particularly to RF signals. EMI can occur in the frequency range commonly identified as "anything greater than DC to daylight."

Radio Frequency (RF). A frequency range containing coherent electromagnetic radiation of energy useful for communication purposes—roughly the range from 10 kHz to 100 GHz. This energy may be transmitted as a byproduct of an electronic device's operation. RF is transmitted through two basic modes:

> *Radiated emissions*. The component of RF energy that is transmitted through a medium as an electromagnetic field. RF energy is usually transmitted through free space; however, other modes of field transmission may occur.
>
> *Conducted emissions*. The component of RF energy that is transmitted through a medium as a propagating wave, generally through a wire or interconnect cables.
>
> *Line Conducted Interference (LCI)*. Refers to RF energy in a power cord or AC mains input cable. Conducted signals do not propagate as fields but may propagate as conducted waves.

Immunity. A relative measure of a device or a system's ability to withstand EMI exposure while maintaining a predefined performance level.

> *Electrostatic discharge (ESD)*. A transfer of electric charge between bodies of different electrostatic potential in proximity to each other or through direct contact. This definition is observed as a high-voltage pulse that may cause damage or loss of functionality to susceptible devices. Although lightning differs in magnitude as a high-voltage pulse, the term *ESD* is generally applied to events of lesser amperage and more specifically to events triggered by human beings.

Radiated immunity. A product's relative ability to withstand electromagnetic energy that arrives via free-space propagation.

Conducted immunity. A product's relative ability to withstand electromagnetic energy that penetrates it through external cables, power cords, I/O interconnects, or chassis. EMI may also couple to a chassis, if interconnects are improperly implemented.

Susceptibility. A relative measure of a device, or a system's propensity to be disrupted or damaged by EMI exposure to an incident field or signal. It is the lack of immunity.

Suppression. The process of reducing or eliminating RF energy that exists without relying on a secondary method, such as a metal housing or chassis. Suppression may include shielding and filtering as well.

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1.2 ELEMENTS OF THE ELECTROMAGNETIC ENVIRONMENT

When an EMI problem occurs, the engineer needs to approach the situation logically. A simple EMI model has three elements:

1. There must be a source of energy.
2. There must be a receptor that is upset by this energy when the intensity of the electromagnetic interference is above a tolerable limit.
3. There must be a coupling path between the source and receptor for the unwanted energy transfer.

For interference to exist, all three elements have to be present. If one of the three elements is removed, there can be no interference. It therefore becomes the engineer's task to determine which is the easiest element to remove. Generally, designing a PCB that eliminates most sources of RF interference is the most cost-effective approach (called *suppression*). The source of interference is the active element producing the original waveform. The PCB must be designed to keep the energy developed to only those sections of the assembly that require this energy. The second and third elements tend to be addressed with containment techniques. Figure 1.1 illustrates the relationship between these three elements and presents a list of items associated with each element.

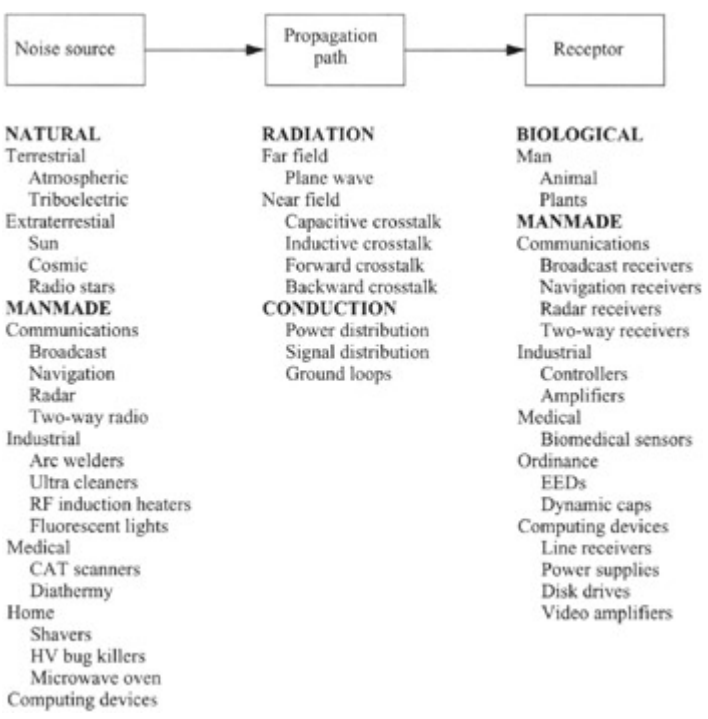

Figure 1.1: Items associated with the three elements of the EMI environment.

With respect to PCBs, observe the following:

- Noise sources are frequency generation circuits, component radiation within a plastic package, incorrect trace routing, ground bounce from digital logic, and common-mode currents developed within an assembly.
- The propagation path is the medium that carries the RF energy, such as free space or interconnects (common impedance coupling).
- Receptors are devices that easily accept interference from I/O cables,

or by radiated means, transferring this harmful energy to circuits and devices susceptible to disruption.

On the surface, a product must be designed for two levels of performance: one to minimize RF energy exiting an enclosure (emissions), and the other to minimize the amount of RF energy entering (susceptibility or immunity). Both emissions and immunity are transmitted by radiated or conductive means. This relationship is shown in Fig. 1.2. Also, it must be considered that a product must be compatible within itself, i.e., emitting levels must not compromise the performance of sensitive segments within the product.

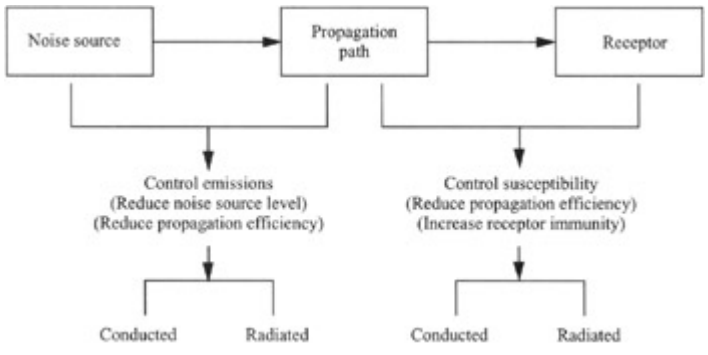

Figure 1.2: Variants of EMI coupling paths.

When dealing with emissions, a general rule-of-thumb is

The higher the frequency, the greater the efficiency of a radiated coupling path; the lower the frequency, the greater the efficiency that a conducted coupling path will cause EMI. The extent of coupling depends on the frequency of the circuit and edge rate transition of digital components switching logic states and transfer mechanism.

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1.3 NATURE OF INTERFERENCE

EMC is grouped into two categories: internal and external. The internal category is the result of signal degradation along a transmission path, including parasitic coupling between circuits in addition to field coupling between internal subassemblies, such as a power supply to a disk drive. Stated more specifically, the problems are signal losses and reflections along the path, along with crosstalk between adjacent signal traces.

External problems are divided into emissions and immunity. Emissions derive primarily from harmonics of clocks or other periodic signals. Remedies concentrate on containing the periodic signal to as small an area as possible, blocking parasitic coupling paths to the outside world.

Susceptibility to external influences, such as ESD or radio frequency interference, is related initially to propagated fields that couple into I/O lines, which then transfer to the inside of the unit, and secondarily to case shielding. The principal recipients are high-speed transmission lines and sensitive adjacent traces, particularly those terminated with edge-triggered components.

There are five major considerations when performing EMC analysis on a product or design [1].

1. *Frequency*. Where in the frequency spectrum is the problem observed?

2. *Amplitude*. How strong is the source energy level, and how great is its potential to cause harmful interference?

3. *Time*. Is the problem continuous (periodic signals), or does it exist only during certain cycles of operation (e.g., disk drive write operation or network burst transmission)?

4. *Impedance*. What is the impedance of both the source and receptor units, and the impedance of the transfer mechanism between the two?

5. *Dimensions*. What are the physical dimensions of the emitting device that cause emissions to occur? RF currents will produce electromagnetic fields that will exit an enclosure through chassis leaks that equal significant fractions of a wavelength or significant fractions of a "rise-time distance." Trace lengths on a PCB have a direct relationship as transmission paths for RF currents.

Whenever an EMI problem is approached, it is helpful to review this list based on product application. Understanding these five items will clear up much of the mystery of how EMI exists within a PCB. Applying these five considerations teaches us that design techniques make sense in certain contexts but not in others. For example, single-point grounding is excellent when applied to low-frequency applications, but it is completely inappropriate for radio frequency signals, which is where most of the EMI problems occur. Many engineers blindly apply single-point grounding for all product designs, without realizing that additional and more complex problems are created using this grounding methodology.

When designing a PCB, we are concerned with current flow within the assembly. Current is preferable to voltage for a simple reason: current always travels around a closed-loop circuit following one or more paths. It

is to our advantage to direct or steer this current in the manner that is desired for proper system operation. To control the path that the current flows, we must provide a low-impedance, RF return path back to the source of the energy. We must also divert interference current away from the load or victim circuit. For those applications that require a high-impedance path from source to the load, consider all possible paths through which the return current may travel.

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1.4 REGULATORY REQUIREMENTS—NORTH AMERICA

Electrical and electronic products generate RF energy. Electromagnetic emission levels are set by rules and regulations mandated by domestic and international governments or agencies. In the United States, the Federal Communications Commission (FCC) regulates the use of radio and wire communications. The FCC is an independent government agency, responsible for ensuring interstate and international communication by radio, television, satellite, and cable.

In Canada, Industry Canada (IC) is the agency responsible for regulating radio and wire communication. Industry Canada performs a function similar to that of the Federal Communications Commission. Harmonized test requirements and standards for North America exist between both the FCC and IC.

The FCC regulates electronic products by specifying technical standards and operational requirements through the Code of the Federal Register (CFR), Title 47. The sections within 47CFR that are most applicable to products discussed herein are Parts 2, 15, 18, and 68. These regulations, developed over many years, are based on complaints filed with the Commission. The most prominent FCC Parts are summarized in the following list. In Canada, the specification equivalent to 47CFR, Part 15, is SOR 88/475.

1. Part 2 is an administrative section that details aspects of how to comply with 47CFR. Included are allocated frequency bands, radio treaty matters, and general rules and regulations. The rules and regulations include registration requirements, authorization procedures, definitions, and various processes to ensure that the federal code is properly administered.

2. Part 15 regulates products that generate unlicensed radio frequency energy, both intentional and non-intentional. Information Technology Equipment (ITE) falls within Part 15.

3. Part 18 regulates Industrial, Scientific, and Medical (ISM) equipment. These devices use radio waves for proper operation.

4. Part 68 regulates electronic equipment connected to a telephone network. This part provides a uniform standard for protecting the telephone network from harm caused by connection of terminal equipment.

The FCC defines a digital device as

> *An unintentional radiator (device or system) that generates and uses timing signal or pulses at a rate in excess of 9,000 pulses (cycles) per second and uses digital techniques; inclusive of telephone equipment that uses digital techniques or any device or system that generates and uses radio frequency energy for the purpose of performing data processing functions, such as electronic computations, operations, transformation, recording, filing, sorting, storage, retrieval or transfer.*

Digital computing products are classified into two categories: Class A and B. The FCC and IC use the same definitions.

Class A: A digital device that is marketed for use in a commercial, industrial, or business environment, exclusive of a device which is marketed for use by the general public or is intended to be used in the home.

Class B: A digital device that is marketed for use in a residential environment, notwithstanding its use in a commercial, industrial, or business environment. Examples of such devices include, but are not limited to, personal computers, calculators, and similar electronic devices that are marketed for use by the general public.

If a product contains digital circuitry and has a clock frequency greater than 9 kHz, it is defined as a digital device and is subject to the rules and regulations of the FCC and IC. Electromagnetic Interference (EMI) may occur as a result of both digital and analog circuits. These products are subject to domestic and international regulatory requirements.

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1.5 REGULATORY REQUIREMENTS—WORLDWIDE

Test requirements, standards, and procedures have been harmonized on a worldwide basis. The principles discussed herein will allow regulatory compliance to be achieved with minimal development cost and shorter design cycles. The harmonization process is based on the work of expert technical committees reporting to the International Electrotechnical Commission (IEC).

The IEC works closely with the International Standards Organization (ISO), which is chartered by the United Nations. Many countries throughout the world are members. The IEC oversees the work of technical committees working on a particular product sector. The IEC's objectives are to "promote international co-operation on all questions of standardization ... achieved by issuing publications including recommendations in the form of international standards."

Two IEC technical committees work on EMC standards. The first is TC77, *Electromagnetic compatibility between equipment including networks*. The second committee is *International Special Committee on Radio Interference* (Comité International Spécial des Perturbations Radioélectriques or CISPR). CISPR publications deal primarily with limits and measurements of the radio interference characteristics of potentially disturbing sources or emissions. CISPR and IEC standards coexist to define most technical aspects related to EMC compliance.

The IEC publications themselves have no legal requirements. National committees do not have to adopt them, although several countries outside of Europe have incorporated them into their national laws. The important aspect of IEC standards is that they have been adopted and harmonized as a European standard for all members of the European Union. Once published as a harmonized document, a legal requirement now exists.

A separate organization, the Committee for European Electrotechnical Standardization (Comité Européen de Normalisation Electrotechnique, or CENELEC), is responsible for developing European standards for electrical equipment. CENELEC received its charter from the Parliamentary Commission of the European Union and produces EMC standards for use with the EMC Directive, usually based on IEC and CISPR publications.

For telecommunications equipment, the European Telecommunications Standards Institute, or ETSI, is the standards-making body. ETSI develops standards for telecommunications network equipment not supplied to the subscriber, in addition to radio communication equipment and broadcast transmitters.

CENELEC and ETSI adopt IEC and CISPR publications, whenever possible, as a basis for preparing a formal standard. The CENELEC committee responsible for preparing EMC standards is TC110. Technical Committee TC110 has several subcommittees, including SC110A, which is responsible for immunity requirements of Information Technology Equipment (ITE).

International EMC publications are commonly referred to as CISPR or IEC, when in fact the real standard, after adoption and publication by the European Commission, is prefixed with an EN (European Normalization) number. To summarize, the European Commission adopts into law requirements developed by CISPR and the IEC, as well as other European

working groups and committees, under the auspices of CENELEC and ETSI.

Although this book focuses on products that fall within the category of ITE, many other product categories can use the information herein. For emission requirements, conducted limits exist from 150 kHz to 30 MHz. Radiated emissions are generally measured from 30 MHz to 1000 MHz, or up to 100 GHz for special products and applications. Immunity tests differ, based on product category, intended end-use environment, and constructional details.

The most commonly referenced CISPR and IEC test publications for products that incorporate printed circuit boards are listed in this section. Appendix B repeats this information with greater detail. Many other test publications and requirements also exist. This list is subject to periodic changes owing to continuing developments in standards writing, along with harmonization within the European Union (EU). The EU was formerly known as the European Community (EC) or the European Economic Community (EEC). This list is current at date of publication and is subject to change without notice. The reader is urged to verify the applicable and current requirements in force at the time of product design and release. For this reason, the year of publication in the *Official Journal of the European Union* (*OJ*), the date of withdrawal, amendment updates, and other supporting information relating to date of publication or implementation are not provided in this book.

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1.6 STANDARDS

Three tiers of standards have been generated: basic standards, generic standards, and product family standards.

1.6.1 Basic Standards

Basic standards are referenced within generic and product family standards as a basis for performing a particular test. The standards include most IEC and CISPR standards and are dedicated to aspects of EMC that are of general interest to what all committees are working on, creating, or developing other standards. This development work includes product family standards. It is common for a product family standard to take the appearance of a generic standard. Specific operational modes and configurations are detailed in the standard, including performance criteria and test levels.

1.6.2 Generic Standards

Generic standards were developed for industry sectors for which no product family standard is available. Generic standards encompass all environments and applications, and are intended to represent the essential requirements of a directive. These standards are divided into two basic requirements: emissions and immunity. Environments are defined as residential, commercial, light industrial, or heavy industrial.

When a relevant product family standard is not available, generic standards take precedent. Regarding product categories, a particular device might have a product family emissions standard and yet be required to use a generic standard for immunity tests. The reason for this is that specific test requirements for immunity may be in the development stage or not yet published in the *OJ*.

Generic Standards (Sample List)

Part 1: Residential, Commercial, and Light Industry

EN 50081-1	Electromagnetic compatibility—Generic emission standard.
EN 50082-1	Electromagnetic compatibility—Generic immunity standard.

Part 2: Industrial Environment

EN 50081-2	Electromagnetic compatibility—Generic emission standard.
EN 50082-2	Electromagnetic compatibility—Generic immunity standard.

Part 3: Special Environment

EN 50081-3	Electromagnetic compatibility—Generic emission standard.
EN 50082-	Electromagnetic compatibility—Generic immunity

 standard.

1.6.3 Product Family Standards

Product family standards take precedence over generic and basic standards after they are published in the *Official Journal of the European Union*. These standards may be specifically designed to cover a particular aspect of EMC for a particular product, or product family, such as Information Technology Equipment (ITE) or Industrial, Scientific, and Medical Equipment (ISM). In addition, product family standards may be created as an addendum to existing product performance standards.

Product family standards refer to internationally adopted basic standards, such as the IEC 1000-4-X or EN 55024 series for immunity test requirements. These requirements define what tests are to be performed, test levels or limits, operational conditions, and performance criteria. Product family standards are generally based on input from professional engineers and companies who specialize within a particular industry. Companies generally have a more comprehensive concept of the EMC environment than does a technical committee. Working together, industrial and technical committees are best suited to developing realistic test procedures and methodologies to meet the essential requirements of the EMC directive.

The development of product family standards is a never-ending process. Frequent changes are made either with an addendum or with a new release. Whenever a standard is released for draft review, adopted, or published in the *Official Journal*, a date is provided next to the standard number, such as EN 55022:1995. When use of standards is required for compliance purposes, one should refer to the latest edition or release date appropriate for the product using a reliable source, such as the European Union's web page. Amendments may or may not be applicable to a particular product being certified.

1.6.4 Classification of ITE Products

Products are classified into two categories for emissions: Class A and B. The definition provided by CISPR 22, which is identical to EN 55022 for ITE follows verbatim. Most products described within the present book fall within this definition [2].

Information Technology Equipment (ITE). Any equipment

a. Which has a primary function of either (or a combination of) energy storage, display, retrieval, transmission, processing, switching, or control of data and of telecommunication messages and which may be equipped with one or more terminal ports typically operated for information transfer;

b. With a rated supply voltage not exceeding 600 V.

ITE includes, for example, data processing equipment, office machines, electronic business equipment, and telecommunication equipment.

Class B ITE. Class B ITE is a category of apparatus, which satisfies the Class B ITE disturbance limits. Class B ITE is intended primarily for use in the domestic environment and may include

- equipment with no fixed place of use; for example, portable equipment powered by built-in batteries;
- telecommunication terminal equipment powered by a telecommunication network;
- personal computers; and auxiliary connected equipment.

Note The domestic environment is an environment in which the use of broadcast radio and television receivers may be expected within a distance of 10 m of the apparatus concerned.

Class A ITE. Class A ITE is a category of all other ITE that satisfies the Class A ITE limits but not the Class B ITE limits. Such equipment should

not be restricted in its sale, but the following warning shall be included in the instructions for use:

Warning This is a Class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

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1.7 EMISSION REQUIREMENTS

The following list deals with emission requirements for the European Union. These standards are identified as product family standards.

Product Family Standards (sample list)

EN 55011	Limits and methods of measurements of radio disturbance characteristics of industrial, scientific, and medical (ISM) radio frequency equipment (CISPR 11).
EN 55013	Limits and methods of measurements of radio disturbance characteristics of broadcast receivers and associated equipment (CISPR 13).
EN 55014	Limits and methods of measurements of radio disturbance characteristics of household electrical appliances, portable tools, and similar electrical apparatus (CISPR 14).
EN 55015	Limits and methods of measurements of radio disturbance characteristics of electrical lighting and similar equipment (CISPR 15).
EN 55022	Limits and methods of measurements of radio disturbance characteristics of Information Technology Equipment (CISPR 22).
EN 55024	Information Technology Equipment—Immunity characteristics—Limits and methods of measurement (CISPR 24).
EN61000-3-2	Harmonic Current Emissions.
EN61000-3-3	Voltage Fluctuations and Flicker in low-voltage supply systems.

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1.8 IMMUNITY REQUIREMENTS

To be able to certify compliance to the EMC Directive, 89/336/EEC, manufacturers must construct products that meet not only emissions requirements, but also immunity levels, or protection against harmful disruption from other electronic equipment. Currently, only Europe requires immunity testing. Since the IEC and CISPR are international organizations, the scope of their work is used throughout the world. CENELEC adopts basic standards developed by both IEC and CISPR, and publishes them as harmonized standards to meet the EMC Directive. The European harmonized document and IEC publication numbers are similar. The IEC standard is prefixed with IEC 1000-4-X. When referenced as a European harmonized document, this number is changed to EN 61000-4-X.

International IEC standards for immunity are provided in the IEC 1000-4-X series. This series of standards describes the test and measurement methods detailed within the basic standards. Basic standards are specific to a particular type of EMI phenomenon, not a specific type of product. This series covers the following:

- Terminology
- Descriptions of the EMI phenomenon
- Instrumentation
- Measurement and test methods
- Ranges of severity levels with regard to the immunity of the equipment

The international IEC 1000-X series of standards, the most commonly used immunity standards adopted or recommended by CENELEC, were reissued using an EN 61000-X specification number. The EN 61000-4-X series of immunity specifications are as follows:

Comprehensive List of Immunity Standards

Standard	Description
EN 61000-4-2	Electrostatic discharge (ESD)
EN 61000-4-3	Radiated electromagnetic field
EN 61000-4-4	Electrical Fast Transient (EFT)/Burst
EN 61000-4-5	Surge
EN 61000-4-6	Conducted disturbance by RF fields
EN 61000-4-7	General guide on harmonics and interharmonics measurements and instrumentation (not a standard; procedure only)
EN 61000-4-8	50/60 Hz magnetic field

EN 61000-4-9	Pulsed magnetic field
EN 61000-4-10	Oscillatory magnetic field
EN 61000-4-11	Voltage dips and interruption
EN 61000-4-12	Oscillatory waves "ring wave"
EN 61000-4-13	Oscillatory waves 1 MHz
EN 61000-4-14	Harmonics, interharmonics, and main signaling
EN 61000-4-15	Voltage fluctuations
EN 61000-4-27	Unbalance in three-phase mains
EN 61000-4-28	Variation of power frequency

Note Several EN 61000-4-x specifications have never been written or released. Titles have been issued and working groups assigned. When performing compliance testing, verify which standards are mandatory for your product along with required test levels and performance criteria.

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1.9 ADDITIONAL REGULATORY REQUIREMENTS—NORTH AMERICA

Other agency requirements in North America include those listed in Table 1.1. These standards are very specific and beyond the scope of this design guideline. A sample list is presented, given that printed circuit boards are used in products covered by these standards.

Table 1.1: Additional North American Standards

Open table as spreadsheet

Standard	Subject Area
SAE Standard SAE J 551	Radiated EMI from vehicles and associated devices.
NACSIM 5100 (a.k.a. Tempest)	Classified standard. This requires emissions from certain products to be sufficiently low to prevent interception and deciphering data streams that contain intelligence.
MIL-STD-461/462	U.S. military standard and test procedure for both radiated and conducted emissions.

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1.10 SUPPLEMENTAL INFORMATION

In addition to EMC compliance, requirements exist for product safety. These requirements include energy hazards and flammability. All printed circuit boards are subject to high voltage and current levels that pose a possible shock hazard to the user. In addition, extensive current flow on traces generates heat, which can cause the fiberglass material used in the construction of the printed circuit board to burn or melt with an associated risk of fire. Components and interconnects placed on a printed circuit board also provide a source of fuel (combustionable material) that may contribute to a fire hazard under abnormal fault conditions.

The Appendixes of this book are an important part of this design guideline. Much technical information is contained in all chapters. To assist during the design and layout of a PCB, Appendix A, Summary of Design Techniques, provides a brief overview of items discussed, cross-referenced to their respective chapter. This summary may be used for quick review during the layout and design stage.

Appendix B is provided as a quick reference to international EMC specification limits for the United States and Canada (FCC/IC), Europe, and worldwide, in addition to the European immunity limits. Appendix C discusses the decibel as well as issues related to using this unit of measurement. Finally, Appendix D presents common conversion tables.

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[1] Gerke, D., and W. Kimmel. 1994. "The Designer's Guide to Electromagnetic Compatibility." *EDN* (January 20).

[2] EN 55022:1995 (CISPR 22:1993). *Limits and methods of measurement of radio disturbance characteristics of information technology equipment.*

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Chapter 2: Printed Circuit Board Basics

OVERVIEW

Developing products that will pass legally required EMC tests is not as difficult as one might expect. Engineers often strive to design elegant products. However, elegance sometimes must be redefined to include product safety, manufacturing, cost, and, of course, regulatory compliance. Such abstract problems can be challenging, particularly if engineers are unfamiliar with design or manufacturing procedures outside their specialized field of engineering. This chapter examines only EMC-related aspects of a PCB and areas of concern during the design cycle.

When designing any electrical product, regardless of complexity, various issues must be addressed. This chapter examines why we need to incorporate design techniques for EMC compliance. Understanding basic concepts will help implement the techniques presented later. When we don't understand fundamental concepts, we end up following rules-of-thumb blindly without knowing why each technique works or whether the technique is even appropriate or required for a particular design or application.

The fundamental concepts examined in this chapter are

1. Hidden characteristics of passive components.
2. How and why RF energy is developed within the PCB.
3. Magnetic flux and cancellation requirements.
4. Routing topology configurations.
5. Layer stackup assignment.
6. Radial migration.
7. Common-mode and differential-mode currents.
8. Grounding methodologies.
9. The need for an optimal return path for RF current.
10. Aspect ratios.
11. Image planes and their use, including discontinuities.
12. Partitioning.
13. Unpublished information related to digital logic selection.

It is desirable to initially suppress RF energy internal to the PCB rather than rely on containment by a metal chassis or electrically conductive plastic enclosure. The use of planes, voltage, or ground (sometimes called "image planes") internal to the assembly is one important design technique of suppressing common-mode RF energy developed within the PCB. In addition to use of planes to control RF energy, proper implementation of decoupling and bypass capacitors for a specific application is required. Capacitor usage is detailed in Chapter 3.

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2.1 HIDDEN RF CHARACTERISTICS OF PASSIVE COMPONENTS

Traditionally, EMC has been considered "the art of black magic." In reality, EMC can be explained by complex mathematical concepts. Some of the relevant equations and formulas are complex and are beyond the scope of this book. Even if mathematical analysis is applied, the equations become too complicated for practical applications. Fortunately, simple models can be formulated to describe how, but do not directly explain why EMC compliance can be achieved. We must remove the mystery from the "Hidden Schematic" syndrome [2].

Many variables exist that cause EMI because EMI is often the result of exceptions to the normal rules of passive component behavior. A *resistor* at high frequency acts as a series combination of inductance within the leads of the resistor, in parallel with a capacitor across the two terminals. A *capacitor* at high frequency acts as an inductor with a resistor in a series combination on each side of the capacitor plates. An *inductor* at high frequency performs as an inductor with a capacitor across the two terminals, along with some resistance in the leads. The expected behavior of passive, discrete components for both high and low frequencies is illustrated in Fig. 2.1.

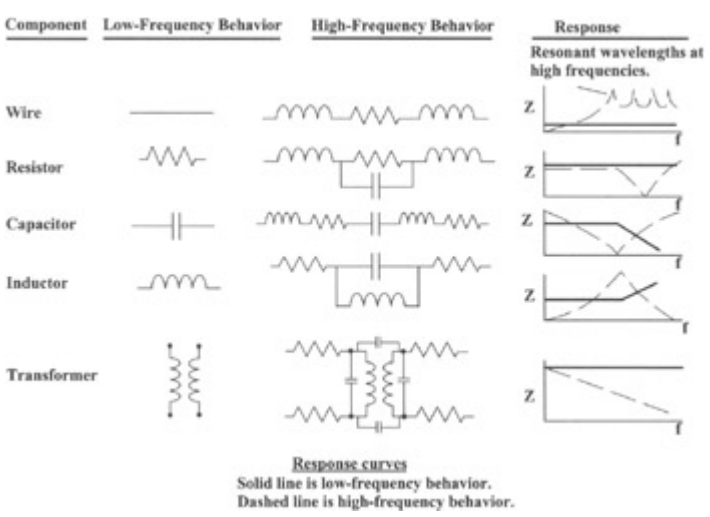

Figure 2.1: Component characteristic at RF frequencies.

Capacitance is always present between two leads. A capacitor is defined as two parallel plates with a dielectric material separating the two plates. For resistors and inductors, the dielectric is usually air. The terminals contain electric charges, the same as if these leads were parallel plates. Thus, for any device, whether it is between the leads of a component, between a component and metal structure (chassis), a PCB and a metal enclosure, or *any* electrical item, relative to another electrical item, parasitic capacitance will be present. We frequently forget that air is a dielectric. Propagation of RF waves usually occurs through free space, or air.

For example, when designing with passive components, we must ask ourselves, "Why is a capacitor not a capacitor?" The answer is simple. The capacitor does not function as a capacitor because it has changed its functional (operational) characteristics, when viewed in the frequency domain. The capacitor will act as an inductor, owing to lead inductance at frequencies above self-resonance. Chapter 3 presents details on capacitor usage. These details include why lead inductance is a major concern in today's products. One cannot select a capacitor using low-frequency

characteristics and then expect it to be a perfect component when RF energy, which is a high-frequency component, is impressed across the terminals.

Conversely, "Why is an inductor not an inductor?" An inductor changes its magnitude of impedance due to parasitic capacitance at high frequencies, which occurs between the two leads and each individual windings.

To be a successful designer, one must recognize the limitations of passive component behavior. Use of proper design techniques to accommodate for these hidden features becomes mandatory, in addition to designing a product to meet a marketing specification.

Digital engineers generally assume that components have a single-frequency response in the time domain only, or low frequency. Consequently, passive component selection for use in accordance with low-frequency criteria without regard to characteristics exhibited in the high-frequency domain will cause significant functional problems to occur, including EMC compliance. EMI exceptions often develop if the designer bends or breaks the rules of passive component behavior.

To restate the complex problem present, consider the field of EMC as *everything that is not on a schematic or assembly drawing*. This statement explains why the field of EMC is considered the art of black magic.

Once the hidden behavior of components is understood, it becomes a simple process to design products that will pass EMC and signal integrity requirements without difficulty. Hidden component behavior must take into consideration the switching speed of all active components, along with *their* unique characteristics, which also have hidden resistive, capacitive, and inductive elements [12].

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2.2 HOW AND WHY RF ENERGY IS DEVELOPED WITHIN THE PCB

Since hidden behavioral characteristics of passive components exist, we now investigate how RF energy is developed within the PCB. Both passive and active digital components develop unwanted RF energy. The field of EMC is described by a series of complex mathematical formulas identified as Maxwell's equations. These equations are based on the physics of electromagnetics. Maxwell's four equations describe the relationship of both electric and magnetic fields. These equations are derived from Ampere's law, Faraday's law, and two from Gauss's law. The formulas are complex and beyond the scope of this book, and are taught as an upper-division course in electrical engineering at colleges and universities. Excellent reference material is provided in the References section; these works discuss how these integral and differential equations (calculus) are derived, as well as their relationship to both static and time-varying fields.

Knowledge of Maxwell's equations is not a prerequisite to designing a PCB for both signal integrity and EMC compliance. This is the primary reason why a detailed analysis of Maxwell is not presented in this book. What is required is a solid understanding of the fundamental concepts of complex physics, and application of these concepts, to solving difficult problems.

To briefly summarize Maxwell, these equations describe the root causes of how EMI is developed: time-varying currents. Static-charge distributions produce static electric fields, not magnetic fields. Constant current sources produce magnetic fields, not electric fields. Time-varying currents produce both electric and magnetic fields. Static fields store energy. This is the basic function of a capacitor: accumulation of charge and retention. Constant current sources are a fundamental concept for the use of an inductor.

To "overly simplify" Maxwell, his four equations are associated to Ohm's law. The presentation that follows is a simplified discussion that allows us to visualize Maxwell in terms that are easy to understand. Although not mathematically perfect, this presentation concept is useful in presenting Maxwell to those with minimal exposure to EMC theory.

(2.1) **Ohm's Law (time domain)** $V = I * R$ **Ohm's Law (frequency domain)** $V_{rf} = I_{rf} * Z$

Get MathML

where *V* is voltage, *I* is current, *R* is resistance, *Z* is impedance (*R* + *jX*), and the subscript *rf* refers to radio frequency energy.

To relate *Maxwell Made Simple* to *Ohm's law*, if RF current exists in a PCB trace which has an impedance value, an RF voltage will be created that is proportional to the RF current present. Notice that in the electromagnetics model, *R* is replaced by *Z*, a complex quantity that contains both resistance (DC-real component) and reactance (AC-complex component). The important item to note is "impedance." Impedance is the resistance to the flow of energy, in both the time and frequency domains. Voltage and current are metric units of measurements that describe the activity of electrons, electromagnetic potential, electrostatic fields, and the like.

For the standard impedance equation, various forms exist. For a wire, or a PCB trace, Eq. (2.2) is the most applicable impedance equation. Within this

equation, we see both inductive and capacitive reactance.

(2.2) $$Z = R + jX_L + \frac{1}{jX_C} = R + j\omega L + \frac{1}{j\omega C}$$

➡ Get MathML

where XL = $2\pi fL$ (the component in the equation that relates only to a wire or a PCB trace)

Xc = $1/(2\pi fC)$ (not observed or present in a pure transmission line or free space.)

ω = $2\pi f$

When a *component* has a known resistive and inductive element, such as a ferrite bead-on-lead, a resistor, a capacitor, or other device with parasitic (hidden) components, Eq. (2.3) is applicable, as the magnitude change of impedance versus frequency must be considered.

(2.3) $$|Z| = \sqrt{R^2 + jX^2} = \sqrt{R^2 + j(X_L - X_C)^2}$$

➡ Get MathML

For frequencies greater than a few kHz, the value of inductive reactance typically exceeds *R*. Current takes the path of least impedance, *Z*. Below a few kHz, the path of least impedance is resistive; above a few kHz, the path of least reactance is dominant. Because most circuits operate at frequencies above a few kHz, the belief that current takes the path of least resistance provides an incorrect concept of how RF current flow occurs within a transmission line structure or PCB trace.

Each trace has a finite impedance value. Trace inductance is only one reason RF energy is developed within a PCB. Even the lead-bond wires that connect a silicon die to its mounting pads may be sufficiently long to cause RF potentials to exist. Traces routed on a board can be highly inductive, especially traces that are electrically long. Electrically long traces are those physically long in routed length such that the time for the round trip of the signal does not return to the source driver before the next edge-triggered event occurs, when viewed in the time domain. In the frequency domain, an electrically long transmission line (trace) is one that exceeds approximately $\lambda/10$ of the frequency that is present within the trace. If a RF voltage travels through an impedance, we end up with RF current, per Ohm's law. This RF current propagates and can cause noncompliance to emission requirements. These examples help us to understand Maxwell's equations and PCBs in *extremely simple terms*.

Another simplified explanation of how RF energy is developed within a PCB is shown in Figs. 2.2 and 2.3. According to Kirchhoff's and Ampere's laws, a closed-loop circuit must be present if the circuit is to work. Kirchhoff's voltage law states that the algebraic sum of the voltage around any closed path in a circuit must be zero.

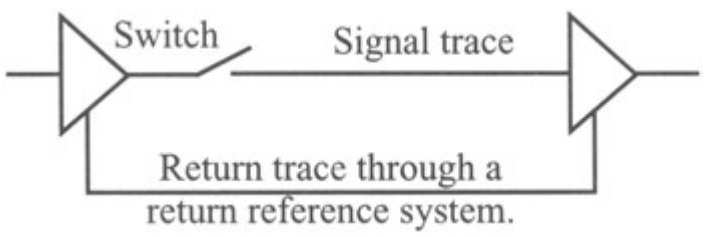

Figure 2.2: Closed-loop circuit.

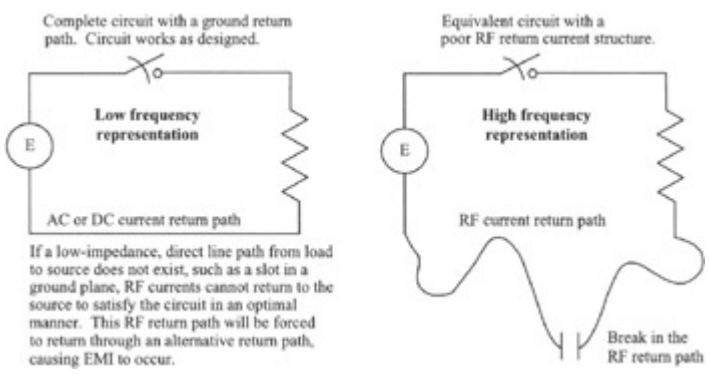
Complete circuit with a ground return path. Circuit works as designed.
Low frequency representation
E
AC or DC current return path
If a low-impedance, direct line path from load to source does not exist, such as a slot in a ground plane, RF currents cannot return to the source to satisfy the circuit in an optimal manner. This RF return path will be forced to return through an alternative return path, causing EMI to occur.
Equivalent circuit with a poor RF return current structure.
High frequency representation
E
RF current return path
Break in the RF return path

Figure 2.3: Frequency representation of a closed-loop

circuit.

Figure 2.2 presents a simplified circuit. There is both a signal path and a return path. Without a closed-loop circuit, a signal would never travel through the transmission line (PCB trace) from source to load. When the switch is closed, the circuit is complete.

Maxwell, Kirchhoff, and Ampere all state that if a circuit is to function or operate, a closed loop must be present. When a trace goes from a source to a load, a current return path must also be present. If a conductive return path is absent, free space becomes the return path.

Figure 2.3 is another representation of Fig. 2.2. The circuit on the left represents a low-frequency network with a direct path for both signal and return current. Every transmission line has a finite impedance value, which consists of both resistance and inductance. For this circuit, the total impedance value is small. Current will return without difficulty. For the circuit on the right, the return path is not the same physical length as the source path. Additional impedance has been added to the transmission line due to this longer path. The longer the trace, the greater inductance becomes. Using the impedance equation, $Z = R + j2\pi fL$, as the *frequency* of the circuit increases, the value of impedance, Z, will increase. With additional *inductance*, total impedance, Z, will also increase. Resistance is negligible for most applications and is usually ignored. For a very high-frequency signal with a significant amount of inductance, the value of Z can become very large. The impedance of free space is 377 ohms. It takes very little inductance, in the frequency range between 100 kHz and 1 MHz, to exceed 377 ohms. Because current (the DC element of the circuit) must return to its source to satisfy Ampere's law, the RF energy (the AC current element) will return through the lowest impedance path available. When the impedance of the return path is greater than 377 ohms, free space becomes the return and is observed as radiated EMI. The illustrations in Fig. 2.3 show both high and low in frequency applicatons.

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2.3 MAGNETIC FLUX AND CANCELLATION REQUIREMENTS

According to Maxwell's equations, when current travels through a transmission line, or PCB trace, magnetic flux is developed. Details on how magnetic fields are developed may be found in the reference material. When a time-variant current (AC waveform) travels down a transmission line, magnetic flux is developed which encircles the transmission line. The magnitude of the current in the transmission line determines the intensity of the magnetic flux.

Magnetic fields exist because a current loop network is present. These fields are radiated through free space as unwanted electromagnetic energy. As can be observed from complex mathematical relationships within Maxwell's equations, time-varying magnetic fields develop electric fields. Like magnetic fields, electric fields also radiate through free space and are the main source of electromagnetic disturbance.

To review *one* fundamental concept regarding how EMI is developed within a PCB, we examine how magnetic flux is created within a transmission line. Magnetic flux is created by a current flowing through an impedance, either fixed or variable. Impedance in a network will always exist within a trace, component bond lead wires, vias, and the like. If magnetic flux is present within a PCB, defined by Maxwell, various transmission paths for RF energy must also be present. These transmission paths may be either radiated through free space or conducted through cable interconnects.

To eliminate RF energy within a PCB, the concept of *flux cancellation* or *flux minimization* needs to be discussed. Although the term *cancellation* is used throughout this book, we may substitute the term *minimization*. Magnetic flux travel is always present within a transmission line. If we bring the RF return path adjacent and parallel to its corresponding source trace, magnetic flux lines observed in the return path (clockwise field), relative to the source path (counterclockwise field), will be in the opposite direction. When we combine a clockwise field with a counterclockwise field, a cancellation effect is observed. If unwanted magnetic flux between a source and return path are canceled or minimized, radiated or conducted RF current cannot exist, except within the minuscule boundary of the transmission line or trace.

The concept of implementing flux cancellation is simple. However, one must be aware of many pitfalls and oversights that may occur when implementing flux cancellation or minimization techniques. With one small mistake, many additional problems will develop. The easiest way to implement flux cancellation is to use image planes, discussed later in this chapter. Regardless of how well we design and lay out a PCB, magnetic and electric fields will always be present. If we minimize magnetic flux, EMI is significantly reduced. It's that simple.

How do we cancel or minimize magnetic flux during a PCB layout? Various techniques are available to the design engineer. A brief summary of some of these techniques is presented below. Not all techniques are involved with flux cancellation/minimization. Although the following items have not yet been discussed, each is described within this book. Among these techniques are:

- Using proper stackup assignment and impedance control for multilayer

boards to allow for a RF return image or ground path to exist.

- Routing a clock trace adjacent to a RF return path, ground plane (multilayer PCB), ground grid, or ground/guard trace (single- and double-sided boards).
- Capturing magnetic flux created internal to a component's plastic package into the 0V-reference system to reduce component radiation.
- Reducing RF currents (energy) within traces by reducing the RF drive voltage from clock or frequency generation circuits, for example, Transistor-Transistor Logic (TTL) versus Complimentary Metal Oxide Semiconductor (CMOS).

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2.4 ROUTING TOPOLOGY CONFIGURATIONS

Two primary topologies are used when designing PCBs: microstrip and stripline; variations on each type exist. Figure 2.4 presents an illustrative overview of these topologies.

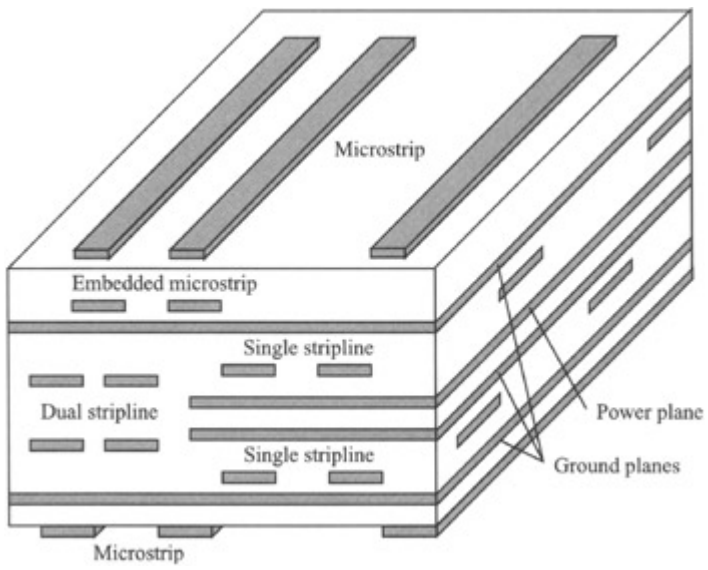

Figure 2.4: Example of a PCB stackup configuration. Note: When using dual stripline, the routing layers are orthogonal, or routed using perpendicular orientation.

2.4.1 Microstrip

Microstrip refers to traces located on the top and bottom, or outer layers of a PCB. Microstrip provides minimal suppression of RF energy that may be created within the PCB. Faster clock and logic signal propagation exists over that of the stripline configuration. These faster signals are due to less capacitive coupling and a lower unloaded propagation delay between source and load. Capacitors are sometimes used on clock signals to slow edge transitions of digital signals. With less capacitive coupling between two solid planes, signals can propagate faster. The drawback of using microstrip is that the outer layers of the PCB can occasionally radiate RF energy to the environment, without the protection of a plane on both sides of this outer circuit layer (Faraday shielding of both the top and bottom sides of the routed traces).

2.4.2 Stripline

Stripline refers to placement of a signal layer between two solid planes: at either voltage or ground potential. Stripline provides for enhanced noise immunity against the propagation of radiated RF emissions, at the expense of slower propagation speeds. Since the circuit (signal) plane is located between solid planes, potential being irrelevant, capacitive coupling will exist. Capacitive coupling between planes slows the edge transition rate of high-speed signals. Capacitive coupling effects within the stripline topology is observed on signals with edge transitions faster than 1 ns. The main benefit of using stripline is complete shielding of RF energy generated from internal traces radiating into free space.

One item to note is that radiation may still occur due to components located on the outer layers of the assembly. Although internal signal traces may not radiate RF energy, bond wires (internal to the component

package), lead frames, sockets, cables, and other interconnects still pose significant problems for the design engineer. Depending on the impedance between interconnects, a mismatch may exist within the transmission line structure. This impedance mismatch may couple RF energy from internal traces to other circuits, or free space, by radiated or conducted means, including crosstalk. Minimizing lead inductance from components on the top layers of the PCB will reduce radiated emissions effects.

A PCB is, in general, a dielectric structure with both internal and external wiring that allows components and interconnects to be mechanically supported and electrically connected together. In addition to providing a mechanism for interconnecting components and connectors, a PCB also provides a medium for component placement. A PCB is a composite of organic and inorganic dielectric material with multiple layers assembled together. Interconnects between layers are by passages, identified as vias. These vias can be plated and filled with metal to provide electrical connection between layers. Solid planar structures provide power and ground to components. Signal lines are distributed among various layers to provide interconnects. An important consideration in the design and specification of a PCB includes both the propagation delay of a transmitted signal and crosstalk between circuits, traces, and interconnects [3].

Board material has become more than just physical support for conductors. Materials used form part of the circuit, dictating length, width, and spacing of traces. It is important to remember that at frequencies above 500 MHz, signal traces become part of the circuit which includes distributed resistance, capacitance, and inductance. At higher frequencies, the dimensions of the transmission line play an important role in defining performance. Changing any dimension can dramatically alter board performance.

An example of physical dimensions related to different routing topologies is presented in Fig. 2.5.

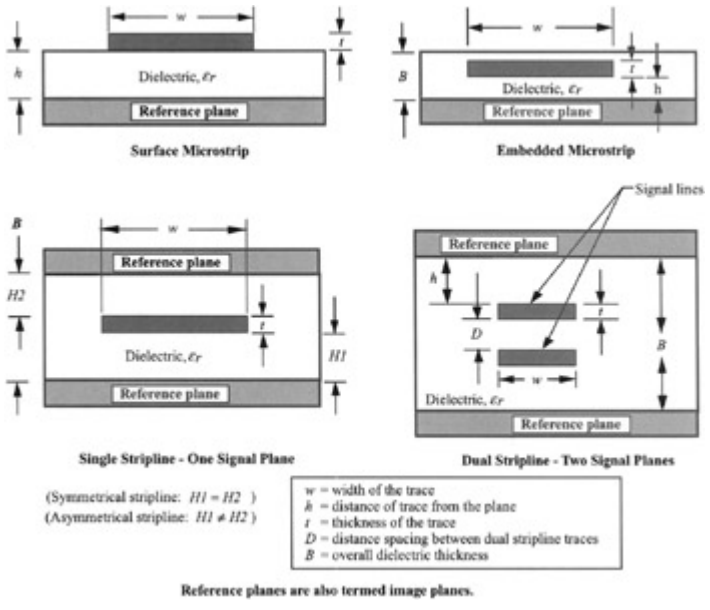

Figure 2.5: Microstrip and stripline topology configurations.

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2.5 LAYER STACKUP ASSIGNMENT

When designing a printed circuit board, a primary consideration is to determine how many routing layers and power planes are required for functionality (within the context of acceptable costs). The number of layers is determined by functional specification, noise immunity (use of power planes), signal category separations, number of nets (traces) to be routed, impedance control, component density of individual circuits, routing of buses, and the like. Proper use of stripline and microstrip topology is required not only for radio frequency (RF) suppression within the PCB, but also for signal integrity purpose. If signal integrity is ensured, no reflections and ringing will result. Thus, emissions will subsequently be reduced, too.

It is desirable to suppress RF energy on the PCB rather than to rely on containment by a metal chassis or conductive plastic enclosure. The use of planes (voltage and ground) embedded in the PCB is one of the most important methods of suppressing common-mode RF energy developed internal to the board. The advantage over most other design techniques is that these planes intrinsically contribute to reducing high-frequency power distribution impedance.

The following stackup assignments are provided only as a guide to determining how to design a multilayer PCB for optimal performance. These assignments are not cast in stone and must be modified as appropriate for functionality reasons, based on the number of routing layers and power/ground planes required. The important thing to notice is that *each and every routing layer is adjacent to a reference (image) plane (power or ground)*, with the exception of the outer microstrip layer and single-sided designs. The outer microstrip layer must contain only slower speed traces without periodic signals or clocks rich in RF spectral energy. A summary of stackup assignments is provided in Table 2.1, at the end of this section.

Table 2.1: Example of Stackup Assignments

Open table as spreadsheet

Stackup	1	2	3	4	5	6	7	8	9	10
2 layers	S1 & ground	S2 & power								
4 layers two routing two planes	S1	ground	power	S2						
4 layers two routing two planes	ground	S1	S2	power						
6 layers four routing two planes	S1	S2	groumd	power	S3	S4				
6 layers four routing two planes	S1	ground	S2	S3	power	S4				
6 layer three routing three planes	S1	power	ground	S2	ground	S3				
8 layers six routing two planes	S1	S2	ground	S3	S4	power	S5	S6		
8 layers four routing four planes	S1	ground	S2	ground	power	S3	ground	S4		
10 layers six	S1	ground	S2	S3	ground	power	S4	S5	ground	S6

routing four planes										
10 layers six routing four planes	S1	S2	power	ground	S3	S4	ground	power	S5	S6
S = signal routing layer										

For the following stackup examples, observe that where three or more reference planes are provided (e.g., one power and two ground planes), optimal performance of high-speed signal traces may be achieved when routed adjacent to a plane at 0V-reference, not adjacent to the power plane. The reason for this statement is one of the basic fundamental concepts of performing EMI suppression techniques within a PCB.

A plane at 0V-potential is generally screw secured to a metal chassis, thus causing this reference plane to be forced at ground potential. If the reference plane is also at ground potential, this reference plane will be unable to change voltage potential levels, which is one cause of ground bounce and board-induced noise voltage. If the 0V-reference plane is tied hard to ground, common in many designs, only the power plane will modulate at switching frequencies of the assembled PCB; thus, this is one less item to worry about.

Research [4] has shown that known IC sources switch significant current within a PCB, relative to the location of the reference planes within a PCB stackup. Capacitive coupling from IC packages to significant metal structures, including heatsinks and nearby shielding enclosures walls, can lead to significant radiated EMI from switching components. This coupling can be exacerbated or minimized by different choices of layer stackup. A ground plane incorporated as the first layer within a multilayer stackup (Layer 2), instead of the power plane, may provide for enhanced suppression of RF energy owing to reduced parasitic capacitive coupling to the enclosure. This consideration must be remembered when assigning a stackup methodology.

2.5.1 Single-Sided Assembly

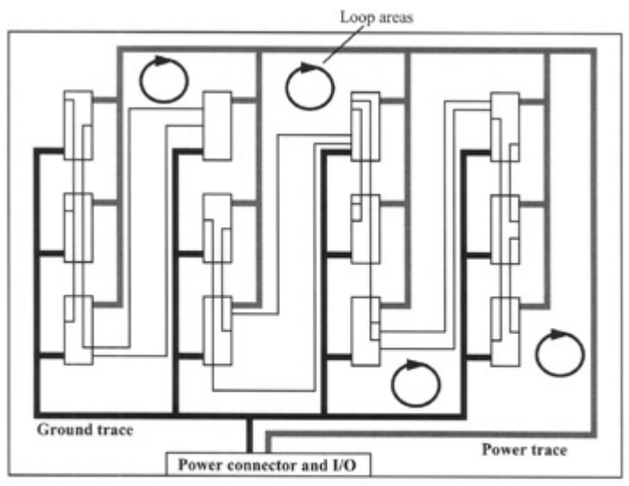
The use of single-sided PCBs is generally reserved to products that do not contain periodic signals (clock) or are designed for use in analog instrumentation and control systems. Because of the limited ability to place components in an optimal manner for short trace lengths, and the need for both a power and ground system, a best case attempt to layout the board must occur.

It is recommended that use of single-sided PCBs be reserved for circuits operating below a few hundred kHz. This low-frequency value is due to various design aspects related to high-frequency circuit requirements, including the applicability of skin effect on traces (traces become highly inductive at high frequencies), the lack of a proper RF return path related to closed-loop circuit requirements, and the need for optimal ground loop control to prevent development of magnetic fields and loop antennas. In addition, single-sided PCBs are highly susceptible to external RF influences such as ESD, fast transient, and radiated/conducted RF susceptibility. The need for termination and layout techniques for signal integrity is not a primary concern, as the edge transition rate is usually not very fast and the physical dimensions of the PCB usually exceed transmission line lengths. In addition, any I/O interconnects will perform beautifully as a radiating antenna, owing to the lack of a RF return path and the need for flux cancellation.

The easiest approach to the design and layout of a single-sided PCB is to begin by developing the power and ground structure (traces). Next come high-threat signals (clocks), which must be routed adjacent to the ground traces as close as physically possible. After these two steps are completed, the rest of the design can be finalized. The following requirements are mandatory:

1. Identify all power and ground sources, along with critical signal nets.
2. Partition the layout into functional subsections. Take into consideration requirements of sensitive components and their physical relationship to I/O ports and interconnects.
3. Position all components with critical signal nets adjacent to each other.
4. If different ground nodes are required, determine if they are to be connected together, and if so, where.
5. Route the rest of the board, keeping in mind the need for flux cancellation for traces rich in RF spectral energy, along with the need for ensuring that a RF return path is available at all time.

Figure 2.6 is the worst type of layout for single-sided designs and should "never" be implemented. This is because excessive loop areas are present within the power and ground distribution network. In addition, no provisions exist for a RF return path for critical traces. Note that this figure shows use of dual-in-line components with the same physical dimensions. In real practice, this type of configuration does not exist, as components with different package sizes and the number and type of traces will always be used. The important item to note is the concept behind *why* this configuration is a very poor layout.



Very poor routing and placement of components for a single-sided design.
Ground loops are excessively large to accommodate for the power and ground traces. Distance routing of the traces are extremely long and must route through the middle of the components—blocked routing paths due to the power and ground traces. Where does one put I/O interconnects for EMC compliance?

Figure 2.6: Single-sided layout—"very poor design concept."

For single-sided PCBs, only one conceptual design technique provides for suppression of RF energy. Asymmetrically placed component package sizes, along with unique power requirements, are becoming standard with today's products. With use of these components, Fig. 2.7 becomes applicable during the design cycle. The

layout topology of Fig. 2.7 is commonly found in analog systems—less than 1 kHz—and in nearly all low-speed, low-technology digital products. Note the use of radial routing of the power and ground traces in the figure versus that of Fig. 2.6.

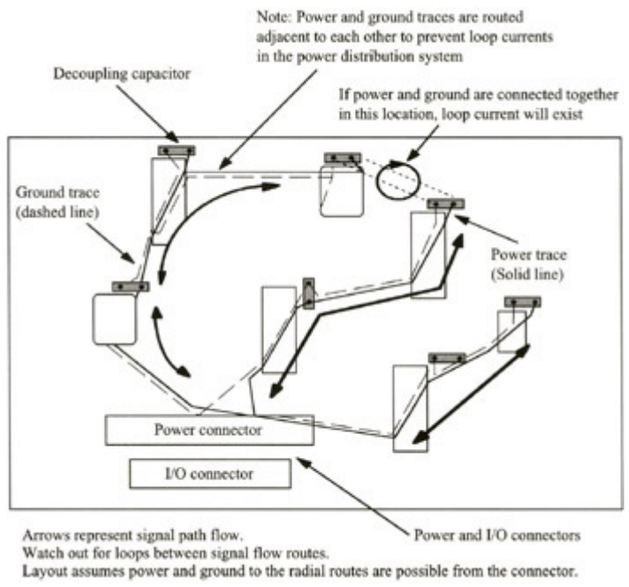

Note: Power and ground traces are routed adjacent to each other to prevent loop currents in the power distribution system
Decoupling capacitor
If power and ground are connected together in this location, loop current will exist
Ground trace (dashed line)
Power trace (Solid line)
Power connector
I/O connector
Power and I/O connectors
Arrows represent signal path flow.
Watch out for loops between signal flow routes.
Layout assumes power and ground to the radial routes are possible from the connector.

Figure 2.7: Single-layer stackup with radial structure for power routing and flow migration.

Radial routing means that all traces emanate from a single-source location. Signal trace routing becomes easier, as direct-line routing is possible, in addition to ease of connection between radial points. The important item to note is that one must not connect the power and ground traces together on the top part of the PCB in the figure. The reason for this requirement is easy to visualize. A ground loop would be created, thus defeating use of radial routing, making this layout appear similar to the one that was shown in Fig. 2.6. The only problem with this layout is to determine how to optimally make the connection to the power connector with different radial structures. The PCB designer must be creative in learning how to implement this technique while maintaining the following for optimal performance:

1. Route all power and ground traces in a radial fashion from the power supply. Minimize total routed length of traces.

2. Route all ground and power traces adjacent (parallel) to each other. This minimizes loop currents that may be created by high-frequency switching noise (internal to the components) from corrupting other circuits and control signals. Ideally, these traces should be separated by a distance greater than the width of any individual trace only when they must be separated for connection to the decoupling capacitor. Signal flow should parallel these return paths.

3. Prevent loop currents by not tying different branches of a tree to another branch.

In Fig. 2.7, the following is to be noted. For a high-frequency application, control the surface impedance (Z) of all signal traces and their return current path. When used in a low-frequency application, instead of attempting to control the impedance of the traces, one must control the topology layout.

2.5.2 Double-Sided Assembly

There are two fundamental layout methodologies for double-sided PCBs. The first is for older technology products (slower speed components) that use Dual-In Line (DIP) packages, located in a straight row or matrix configuration. Very few products use this topology, and they are usually found only in memory arrays. Figure 2.8 illustrates this type of layout. The second configuration is typical of current design practice.

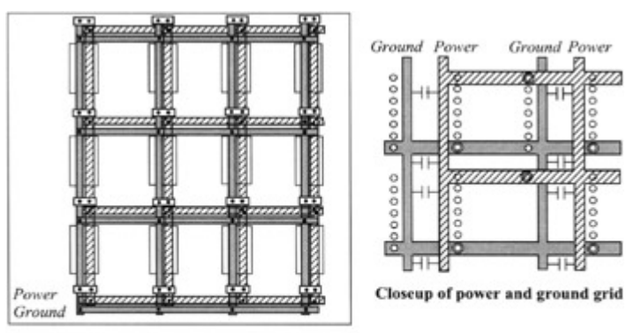

Power
Ground
Ground Power Ground Power
Closeup of power and ground grid
1. Top of board has all vertical traces.
2. Bottom of board has all horizontal traces.
3. Feedthroughs where power and ground traces intersect.
4. Decoupling capacitors between power and ground at connectors and at each IC.
5. Signal lines follow vertical/horizontal pattern.

Figure 2.8: Two-layer PCB with power and ground grid structure.

First Configuration (rarely used) (Fig. 2.8):

- Layer the power and ground in a grid style with the total loop area formed by each grid square not exceeding 1.5 square in. (3.8 square cm).
- Run power and circuit traces at 90-degree angles to each other, power on one layer, ground on the other.
- Place ground traces on one layer—vertical polarization; place power traces on the other layer—horizontal polarization, or vice versa.
- Locate decoupling capacitors between the power and ground traces at all connectors and at each IC.

For Fig. 2.9, a return trace must be placed as physically close to the high-threat signal trace as possible to permit RF energy to complete its return path back to the source. The power and return trace must also be routed parallel to each other, with decoupling capacitors provided for each and every component that injects switching energy into the power distribution system. With this topology, difficulties in routing may occur. However, significant benefits will be achieved, related to EMC compliance.

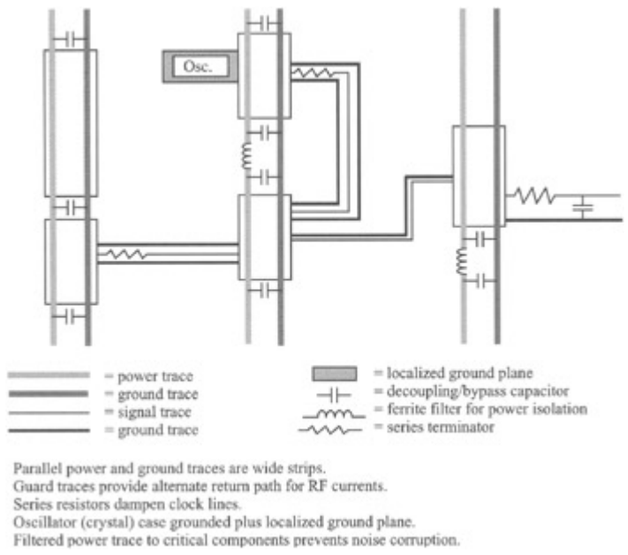

Osc.
= power trace
= ground trace
= signal trace
= ground trace
= localized ground plane
= decoupling/bypass capacitor
= ferrite filter for power isolation
= series terminator
Parallel power and ground traces are wide strips.
Guard traces provide alternate return path for RF currents.
Series resistors dampen clock lines.
Oscillator (crystal) case grounded plus localized ground plane.
Filtered power trace to critical components prevents noise corruption.

Figure 2.9: Enhanced double-sided routing to accommodate RF return currents.

When a gridded power and ground layout methodology is used, care must be taken to guarantee that the grids are tied together in as many places as possible. If a grid is not provided, RF loop currents from components will not find a low-impedance return path by any reliable means, thus exacerbating emissions. Routing power and return traces adjacent to each other, using parallel routes, allows for a low-impedance, small-loop area transmission line structure or antenna to exist. With a small-loop area, the RF energy developed will be at such a high frequency that the signals measured may be in the upper MHz range and thus may not pose problems for EMC compliance. The signal traces referenced to the 0V-return can still create significant current loops, if the distance spacing between the trace and 0V-reference is excessively large.

A problem with double-sided PCBs is how traces are routed between components when a power and ground grid exists. In almost every application, it becomes impractical to fully grid a double-sided board. The most optimal layout technique is to use ground fill to substitute as an alternative return path for loop area control and reduced impedance for RF return currents. This ground fill must be connected to the 0V-reference point in as many locations as possible.

The second layout methodology (Fig. 2.9) for double-sided PCBs is identical to that in Fig. 2.8. The only difference lies in routing of the power and ground traces on both the top and bottom layers. By having two layers available, routing becomes easier to achieve, with loop areas remaining as small as possible.

It is important to note, especially for EMC compliance, that there is *no such thing as a double-sided PCB*, although they physically exist. For example, when analyzing a double-sided stackup related to EMC compliance, with standard thickness of 0.062 in. (1.6 mm), the physical distance spacing between the top layer (with components) and bottom layer (with a ground plane or 0V-reference) is often assumed to provide a return path for RF currents present within the top layer. This is illustrated in Fig. 2.10. In reality, the distance spacing between the signal trace and the return plane is physically large compared to the distance spacing between traces. This large physical distance between trace and plane does not allow for optimal flux cancellation. For this example, the field distribution within the signal trace is approximately one trace width. The physical distance of the field distribution between traces is magnitudes less than the physical distance between trace and reference plane on the opposite side of the PCB. This means that any RF return path that is greater than one trace width distance from the signal source is too far away to perform for *optimal* return flux cancellation, related to the development of RF energy.

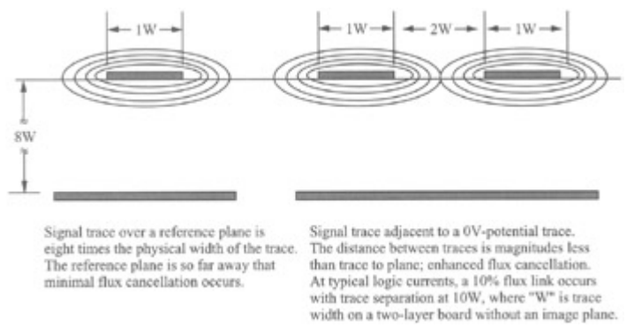

1W
1W
2W
1W
8W
Signal trace over a reference plane is eight times the physical width of the trace. The reference plane is so far away that minimal flux cancellation occurs.
Signal trace adjacent to a 0V-potential trace. The distance between traces is magnitudes less than trace to plane; enhanced flux cancellation. At typical logic currents, a 10% flux link occurs with trace separation at 10W, where "W" is trace width on a two-layer board without an image plane.

Figure 2.10: Example why two-layer stackups are not efficient for removing RF energy.

The best way to approach a double-sided PCB design is to think of the board as two single-sided designs. Route both the top and bottom layers of the PCB using design rules and techniques appropriate for single-sided designs. Ground loop control must be maintained at all times, along with a provision for RF return current to exist.

2.5.3 Four-Layer Stackup

There is only one optimal way to perform a four-layer stackup that works well for EMC compliance, although two configurations are possible, each with two options: symmetrical and asymmetrical. Use of reference planes enhances the ability for flux cancellation of RF currents. The physical distance from the signal layer to reference plane is much less than double-sided boards; hence, radiated RF energy is reduced. A four-layer assembly is still not optimal for flux cancellation of RF currents created by circuits and traces. The reason is the same as for double-sided board—the physical distance spacing between source trace and return path is still excessively large.

Two possible configurations are as follows:

Symmetrical Distance Spacing (Fig. 2.11 top)

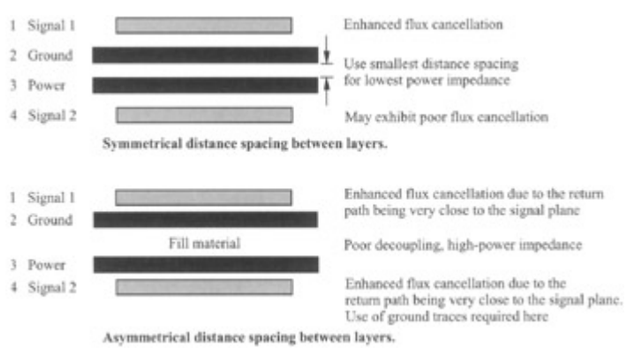

1 Signal 1
2 Ground
3 Power
4 Signal 2
Enhanced flux cancellation
Use smallest distance spacing for lowest power impedance
May exhibit poor flux cancellation
Symmetrical distance spacing between layers.
1 Signal 1
2 Ground
Fill material
3 Power
4 Signal 2
Enhanced flux cancellation due to the return path being very close to the signal plane
Poor decoupling, high-power impedance
Enhanced flux cancellation due to the return path being very close to the signal plane. Use of ground traces required here
Asymmetrical distance spacing between layers.

Figure 2.11: Four-layer stackup assignment—two configurations.

- First layer (component side)—signals and clocks
- Second layer—ground plane

- Third layer—power plane
- Fourth layer (bottom)—signals and clocks

Asymmetrical Distance Spacing (Fig. 2.11 bottom)

- First layer (component side)—signals and clocks
- Second layer—ground plane
- Fill material
- Third layer—power plane
- Fourth layer (bottom)—signals and clocks

These two options present a number of problems.

Symmetrical Stackup

- Signal traces will have a higher impedance, somewhere between 105 and 130 ohms.
- Interplane decoupling to remove switching energy from the power and ground planes is moderate (some benefit).
- RF return currents do not have the ability to return to their source uninterrupted, unless a ground trace is routed on the signal layer adjacent to the power plane.

Asymmetrical Stackup

- Impedance of the routing layers can be specified and set to a desired value.
- Interplane decoupling benefits are basically nonexistent. Extensive use of discrete decoupling capacitors is now required.
- RF return currents do not have the ability to return to their source uninterrupted, unless a ground trace is routed on the signal layer adjacent to the power plane.
- The fill layer (prepreg in this case) is difficult to manufacture at this thickness level.

A second stackup configuration is shown in Fig. 2.12, with the outer layers at power and ground potential, and signal traces routed internally. Use of fill material to make an asymmetrical stackup is also possible, as shown in Fig. 2.11.

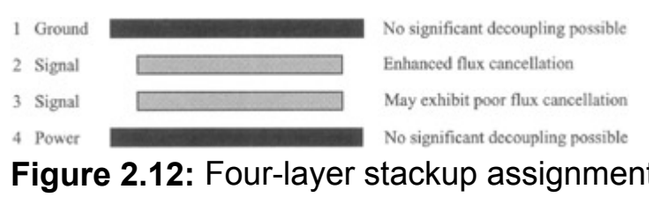


Figure 2.12: Four-layer stackup assignment—alternation configuration.

Planes as Outside Layers

- It is impossible to repair a damaged assembly; it is difficult to test and debug.
- The PCB is difficult to manufacture, as the outer planes function as one large heatsink during the wave-solder process, causing possible cold solder joints to develop. If both layers are at ground potential, then power must be routed as a trace on a signal plane. No decoupling will exist. Extensive use of discrete capacitors is now required.
- RF energy associated with the traces is prevented from radiating to the environment. However, this energy will be transferred to the lead-bond wires of the components located on the outer layers. These components will radiate *all* internal RF energy, if a proper RF return path is not designed into the assembly.

2.5.4 Six-Layer Stackup

Three configurations are commonly found in product designs although other configurations are possible based on intended use and application.

Configuration 1: Six Routing Layers, Two Reference Planes (Fig. 2.13a)

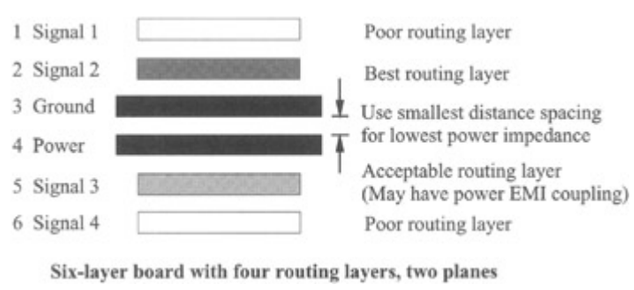


Figure 2.13a: Six-layer stackup assignment—configuration 1.

- First layer (component side)—microstrip routing layer
- Second layer—embedded microstrip routing layer
- Third layer—ground plane
- Fourth layer—power plane
- Fifth layer—embedded microstrip routing layer
- Sixth layer (bottom)—microstrip routing layer

This configuration gives a lower power/ground plane impedance than a four-layer assembly. Having this lower impedance improves overall decoupling for components. The routing plane (Layer 2) adjacent to the ground plane is preferred for routing traces rich with RF spectral energy. Although the alternative routing layer for other high-threat signals, Layer 5, is available, provisions must be made to ensure that a RF return path exists for all traces

routed on Layer 5. The two outer microstrip layers are inappropriate for routing any traces susceptible to an externally induced RF event (e.g., electrostatic discharge, electrical fast transient).

The following is a list of trace impedance values for a PCB stackup with overall thickness of 62 mils (0.062 in. or 1.6 mm) and dielectric constant of 4.3. The routing layers use a symmetrical stackup. Symmetrical stackup means that the distance spacing between all layers is 0.010 in. (10.0 mils or 0.25 mm). The weight of the copper is 1 oz. The impedance values listed are approximate and subject to ±5% tolerance, since different parameters may be used for calculating trace impedance from that shown in the following list. If impedance-controlled transmission lines are required, jumping traces between the outer microstrip and embedded microstrip layers are not advised owing to the extensive impedance mismatch present. Chapter 4 presents the equations that allow us to calculate trace impedance.

Trace Width

5.0 mils–0.005 in. (0.13mm): Outer microstrip—110 Ω, embedded microstrip—79 Ω.

6.0 mils–0.006 in. (0.15mm): Outer microstrip—105 Ω, embedded microstrip—74 Ω.

8.0 mils–0.008 in. (0.20mm): Outer microstrip—97 Ω, embedded microstrip—66 Ω.

10.0 mils–0.010 in. (0.25mm): Outer microstrip—90 Ω, embedded microstrip—60 Ω.

Configuration 2: Six Routing Layers, Two Reference Planes (Fig. 2.13b)

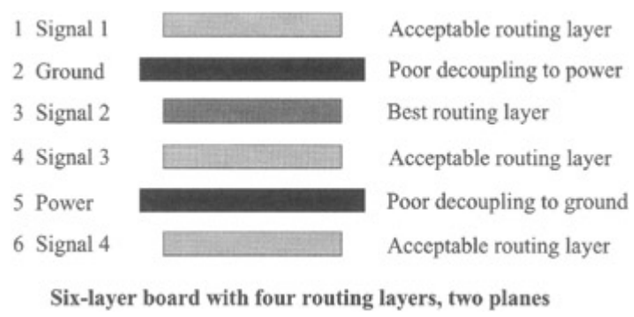


Figure 2.13b: Six-layer stackup assignment—configuration 2.

- First layer (component side)—microstrip routing layer
- Second layer—ground plane
- Third layer—stripline routing layer
- Fourth layer—stripline routing layer
- Fifth layer—power plane
- Sixth layer (bottom)—microstrip routing layer

The advantages and disadvantages of this stackup assignment depend on how the design is to be implemented, along with signal integrity concerns. The advantages include a lower impedance value between routing layers (enhanced signal integrity), along with a shielding effect of the planes from allowing RF energy to propagate to the environment. One disadvantage is that there is practically no decoupling between the power and ground plane. Consequently, a significant number of discrete capacitors will be required, adding material cost along with taking up real estate during placement. Although self-shielding occurs owing to the stripline planes, component radiation will still be present.

An alternative version of Configuration 2 is to provide fill material between Layers 3 and 4 (Signal 2 and 3). By keeping the overall outside dimension constant, the distant spacing between layers must become smaller. A smaller distant spacing between routing layers and a reference plane will reduce the impedance of the transmission line, allowing us to have more closely matched impedance for the transmission lines when jumping layers. The disadvantage of applying fill material is that this extra distance spacing minimizes any benefit from planar decoupling.

The impedance values for Configuration 2, using the same constraints detailed in Configuration 1, are as follows:

Trace Width

5.0 mils–0.005 in. (0.13mm): Outer microstrip—84 Ω, stripline—68 Ω.

6.0 mils–0.006 in. (0.15mm): Outer microstrip—79 Ω, stripline—63 Ω.

8.0 mils–0.008 in. (0.20mm): Outer microstrip—71 Ω, stripline—57 Ω.

10.0 mils–0.010 in. (0.25mm): Outer microstrip—65 Ω, stripline—52 Ω.

Configuration 3: Three Routing Layers, Three Reference Planes (Fig. 2.13c)

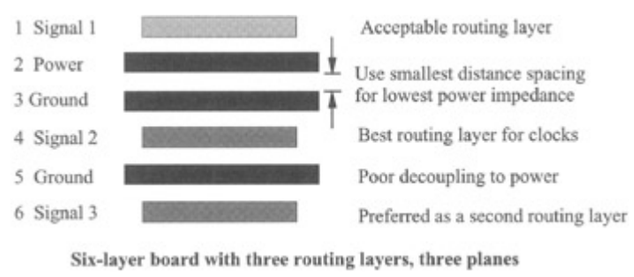


Figure 2.13c: Six-layer stackup assignment—configuration 3.

- First layer (component side)—microstrip routing layer
- Second layer—power plane
- Third layer—ground plane
- Fourth layer—stripline routing plane
- Fifth layer—ground plane

- Sixth layer (bottom)—microstrip routing layer

Configuration 3 is a different type of layer stackup, with three routing planes and three reference planes. This configuration is not realistic owing to the large overhead of solid copper layers (50%). This stackup assignment is far from optimal. It is common practice to construct PCBs with symmetry between layers. The purpose of discussing this stackup arrangement is to illustrate a concept.

Two of the planes in Configuration 3 are at ground potential. One would use this type of topology because there are too many traces to be routed on a four-layer board but not enough to justify four routing layers. With this situation, converting one signal plane to a ground plane has significant advantages, especially enhanced decoupling capabilities and lower transmission line impedance. With two ground planes (Layers 3 and 5), high-threat signals (clocks) must be routed on Layer 4. With this configuration, a coaxial transmission line structure is present, which is optimal for signal integrity and suppression of EMI energy.

If Layers 2 and 3 were swapped, with the power plane in the middle of the board, one feature would become noticeable. Two different sets of decoupling capacitor are now present, each with a different self-resonant frequency and level of performance. The disadvantage of this configuration lies in having the routing layer sandwiched between two planes of different polarities, which minimizes optimal RF return current flow. RF current can now only jump layers at a location where decoupling capacitors are located. Component radiation still occurs.

Impedance values for Configuration 3, using the same constraints detailed in Configuration 1, are presented in the following list. Notice that the impedance of all routing layer is less, which is desired for signal integrity concerns, if layer jumping occurs or signal integrity issues are important.

Trace Width

5.0 mils–0.005 in. (0.13mm): Outer microstrip—84 Ω, stripline—59 Ω.

6.0 mils–0.006 in. (0.15mm): Outer microstrip—79 Ω, stripline—55 Ω.

8.0 mils–0.008 in. (0.20mm): Outer microstrip—71 Ω, stripline—49 Ω.

10.0 mils–0.010 in. (0.25mm): Outer microstrip—65 Ω, stripline—44 Ω.

2.5.5 Eight-Layer Stackup

Many configurations exist. There are two types of assignments that are widely used, presented herein. Not every possible stackup configuration can be presented. The concepts detailed within the six-layer section must be understood and extrapolated to fit the designer's requirements. The first configuration provides for minimal EMI suppression. The second configuration provides maximum suppression owing to the use of an additional solid plane and enhanced flux cancellation for RF currents. Determination of whether to use Configuration 1 or 2 depends on the number of nets to be routed, component density (pin count), buss structures, analog and digital circuitry, and available real estate.

Configuration 1: Six Routing Layers, Two Reference Planes (Fig. 2.14a)

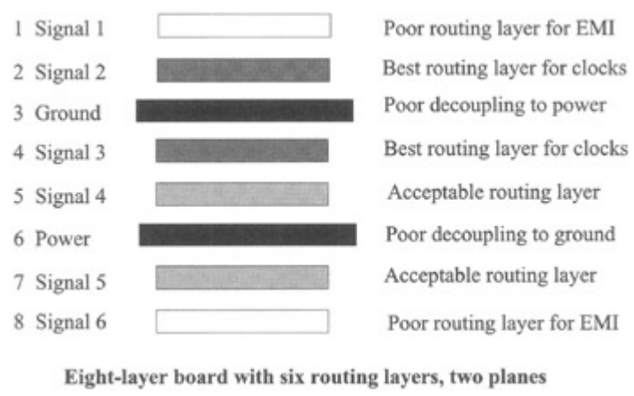


Figure 2.14a: Eight-layer stackup, configuration 1.

- First layer (component side)—microstrip routing layer
- Second layer—embedded microstrip routing layer
- Third layer—ground plane
- Fourth layer—stripline routing layer
- Fifth layer—stripline routing layer
- Sixth layer—power plane
- Seventh layer—embedded microstrip routing layer
- Eighth layer (bottom)—microstrip routing layer

This configuration is not an optimal stackup for several reasons. Designers who need six routing layers will use this methodology because it is the only one available. Disadvantages lie in very poor decoupling, layer jumping between reference planes with different polarities, and two microstrip layers on each side which can radiate RF energy. The optimal layers to route clock and high-threat signals are Layers 2 and 4 (Signal 2 and Signal 3). This is required is because traces rich with RF spectral energy will have a continuous RF return path to complete the closed-loop requirements against the *same* reference plane. Although one can route clocks on Layer 5 (Signal 4), RF return current will bounce between the power and ground planes, which may exacerbate development of RF energy. Because flux cancellation occurs between a signal plane and reference plane, an embedded microstrip layer will not radiate any more than a trace routed stripline with RF energy transferred through vias. Transference of RF energy through vias allows components to pick up the energy and radiate as EMI.

Impedance values for this eight-layer stackup are listed in the following, with the exception that the distance spacing between layers is 7.0 mils (0.007 in. or 0.028 mm) in order to maintain an overall thickness of 62 mils (0.062 in. or 1.6 mm). Notice that the impedance of the embedded microstrip and stripline layers is closer in value, which enhances signal integrity. The impedance of the outer microstrip layer is very high, and should not be used for routing impedance-controlled or high-threat signal traces, including clocks.

Trace Width

5.0 mils–0.005 in. (0.13mm): Outer microstrip—99 Ω, embedded microstrip—68 Ω, stripline—58 Ω.

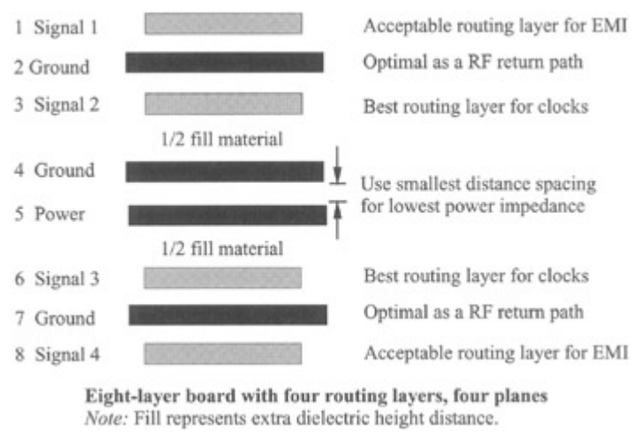
6.0 mils–0.006 in. (0.15mm): Outer microstrip—94 Ω, embedded microstrip—63 Ω, stripline—54 Ω.

8.0 mils–0.008 in. (0.20mm): Outer microstrip—86 Ω, embedded microstrip—55 Ω, stripline—48 Ω.

10.0 mils–0.010 in. (0.25mm): Outer microstrip—79 Ω, embedded microstrip—50 Ω, stripline—43 Ω.

The next stackup assignment is excellent for both signal integrity and EMC.

Configuration 2: Four Routing Layers, Four Reference Planes (Fig. 2.14b)



Eight-layer board with four routing layers, four planes
Note: Fill represents extra dielectric height distance.

Figure 2.14b: Eight-layer stackup, configuration 2.

- First layer (component side)—microstrip routing layer
- Second layer—ground plane
- Third layer—stripline routing layer
- Fourth layer—ground plane
- Fifth layer—power plane
- Sixth layer—stripline routing layer
- Seventh layer—ground plane
- Eighth layer (bottom)—microstrip routing layer

The advantages of using this stackup assignment lie in excellent decoupling (low power/ground impedance) and enhanced flux cancellation (minimization). The fill material is extra thickness added to the assembly. This separation distance forces magnetic flux on Layer 6 (Signal 3) to be captured by the ground plane and not the power plane; it allows for an optimal RF return path to exist. The disadvantage of this stackup is that various impedance values are present, which may be harmful for signal integrity concerns if layer jumping occurs between the microstrip and stripline layers. As detailed in the figure, Layers 3 and 6 (Signals 2 and 3) have almost the same impedance. Hence, both routing layers are excellent for signal integrity and RF flux cancellation; it is the best possible configuration.

Impedance values for this eight-layer stackup, using the same constraints detailed in Configuration 1, are presented in the following list, with the exception that the distance spacing between layers has to be modified. Distance spacing between layers is now at 7.0 mils (0.007 in. or 0.028 mm). The fill material between the power plane (Layer 5) and Signal 3 (Layer 6) is 10.0 mils thick—0.010 in., or 0.25 mm. With this additional thickness, distance spacing between the power and ground plane is reduced to 4 mils—0.006 in. (0.13 mm). This distance modification allows us to maintain an overall thickness of 62 mils (0.062 in. or 1.57 mm).

Trace Width

5.0 mils–0.005 in. (0.13mm): Signals 1 and 4—72 Ω, Signal 2—50 Ω, Signal 3—54 Ω.

6.0 mils–0.006 in. (0.15mm): Signals 1 and 4—68 Ω, Signal 2—46 Ω, Signal 3—50 Ω.

8.0 mils–0.008 in. (0.20mm): Signals 1 and 4—60 Ω, Signal 2—40 Ω, Signal 3—44 Ω.

10.0 mils–0.010 in. (0.25mm): Signals 1 and 4—54 Ω, Signal 2—35 Ω, Signal 3—39 Ω.

2.5.6 Ten-Layer Stackup

Having presented detailed discussion on six- and eight-layer stackup assignments, we see that the same fundamental principles exist with ten or more layers. With a larger stackup, improvement in impedance control and RF flux cancellation is observed. The discussion on higher stackup assignments follows the same concepts presented in this section.

Two sample configurations are detailed for a ten-layer stackup. These two assignments have the same number of routing and reference planes, except for the physical placement of the planes. The important item to note is the physical location of the routing plane relative to a reference plane (at 0-V potential), along with enhanced impedance control.

Configuration 1: Six Routing Layers, Four Reference Planes (Fig. 2.15a)

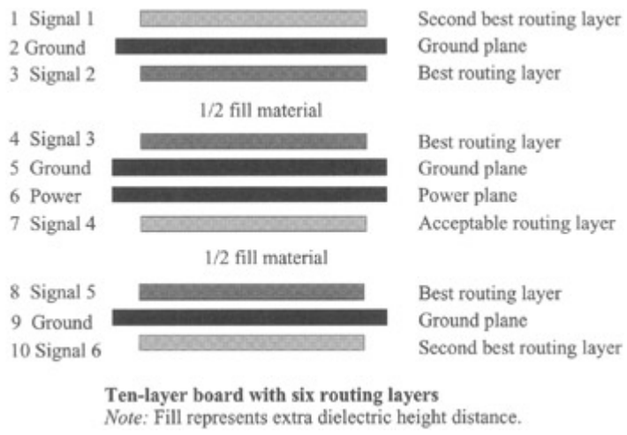


Figure 2.15a: Ten-layer stackup, sample configuration.

- First layer (component side)—microstrip routing layer
- Second layer—ground plane
- Third layer—stripline routing layer
- Fourth layer—stripline routing layer
- Fifth layer—ground plane
- Sixth layer—power plane
- Seventh layer—stripline routing layer
- Eighth layer—stripline routing layer
- Ninth layer—ground plane
- Tenth layer (bottom)—microstrip routing layer

Impedance values for this ten-layer stackup is shown in the following listing. Distance spacing between all layers is 5.0 mils–0.005 in. (0.13 mm), while the fill is 8.0 mils (0.008 in. or 0.20 mm). The distance between the power and ground plane pair is 4.0 mils–0.004 in. (0.10 mm). This stackup is based on a 62 mil (0.062 in. or 1.6 mm) thick PCB. Ten-layer PCBs are generally built at the next standard thickness of 93 mils (0.093 in. or 2.4 mm).

Impedance calculations for a 93 mil thick PCB is not provided for this particular stackup example. The fill material in Fig. 2.15 illustrates a concept, although use of fill is usually not required, or desired, for this particular example.

Trace Width

5.0 mils–0.005 in. (0.13mm): Outer microstrip—99 Ω, embedded microstrip—68 Ω, stripline—58 Ω.

6.0 mils–0.006 in. (0.15mm): Outer microstrip—94 Ω, embedded microstrip—63 Ω, stripline—54 Ω.

8.0 mils–0.008 in. (0.20mm): Outer microstrip—86 Ω, embedded microstrip—55 Ω, stripline—48 Ω.

10.0 mils–0.010 in. (0.25mm): Outer microstrip—79 Ω, embedded microstrip—50 Ω, stripline—43 Ω.

Configuration 2: Six Routing Layers, Four Reference Planes (Fig. 2.15b)

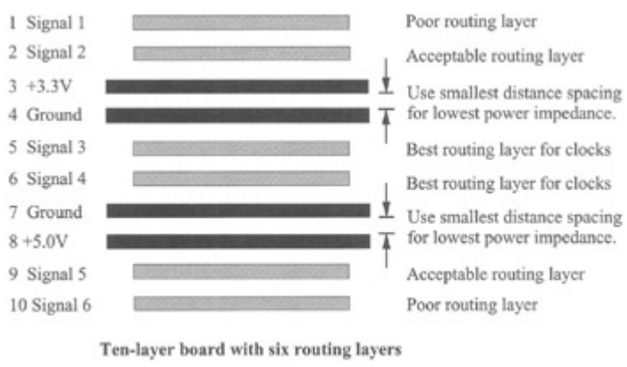


Figure 2.15b: Ten-layer stackup, sample configuration.

- First layer (component side)—microstrip routing layer
- Second layer—embedded microstrip routing layer
- Third layer—+3.3V power plane
- Fourth layer—ground plane
- Fifth layer—stripline routing layer
- Sixth layer—stripline routing layer
- Seventh layer—ground plane
- Eighth layer—+5.0V power plane
- Ninth layer—embedded microstrip routing layer
- Tenth layer (bottom)—microstrip routing layer

The advantage of this stackup assignment lies in having two optimal routing layers for clock and other high-threat signal traces. By locating the power and ground planes in the order shown, Layers 5 and 6 are surrounded by two ground planes. This structure simulates a coaxial cable. Decoupling effects are now available for two separate voltage sources.

Impedance values for this ten-layer stackup is shown in the following list. Distance spacing between all layers is 5.0 mils–0.006 in. (0.13 mm). This stackup is based on a 62 mil (0.062 in. or 1.57 mm) thick PCB. Ten-layer PCBs are generally built at the next standard thickness of 93 mils (0.093 in. or 2.4 mm).

Trace Width

5.0 mils–0.005 in. (0.13mm): Outer microstrip—88 Ω, embedded microstrip—58 Ω, stripline—50 Ω.

6.0 mils–0.006 in. (0.15mm): Outer microstrip—84 Ω, embedded microstrip—53 Ω, stripline—46 Ω.

8.0 mils–0.008 in. (0.20mm): Outer microstrip—75 Ω, embedded microstrip—46 Ω, stripline—40 Ω.

10.0 mils–0.010 in. (0.25mm): Outer microstrip—69 Ω, embedded microstrip—41 Ω, stripline—35 Ω.

Table 2.1 summarizes these stackup assignments for quick reference.

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2.6 RADIAL MIGRATION

Radial migration deals with the transfer of electromagnetic energy from a high-bandwidth section, such as a central processing unit (CPU) or frequency-generating circuits, to lower speed sections, which include I/O interconnects (Fig. 2.16). Radial migration signifies that as the energy from one circuit progress from a high-bandwidth area to a low-bandwidth area, the signal will observe an intrinsic propagation delay. This slowing of signal propagation occurs because all components have input capacitance along with an internal propagational delay. Each device thus slows the edge rate transition (*tr*) of the propagated signal. In addition, slower speed components are generally provided for I/O interconnects. With high-technology products, including networking and graphical interfaces, the concept of radial migration is generally ignored, as high-bandwidth components are required everywhere, especially in the I/O section. As circuits cascade from the CPU area to I/O, one can sum up delays (like a filter) until the high-bandwidth spectral components are slowly decreased from the system and I/O circuits.

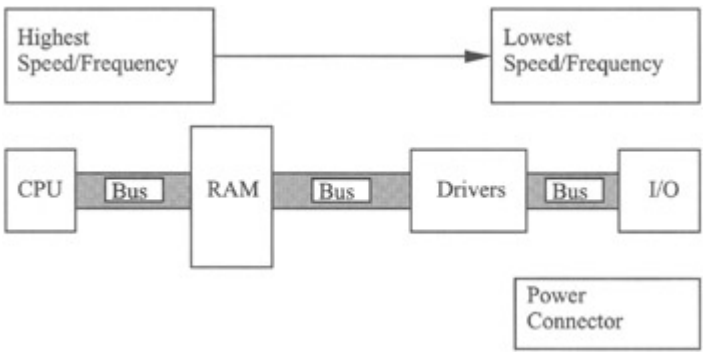

Figure 2.16: Radial migration concept.

An easier way of visualizing radial migration is shown in Fig. 2.17. This figure illustrates how the overall concept of radial migration applies to a PCB and how it relates to partitioning sections of the design into functional areas. Partitioning is discussed later within this chapter.

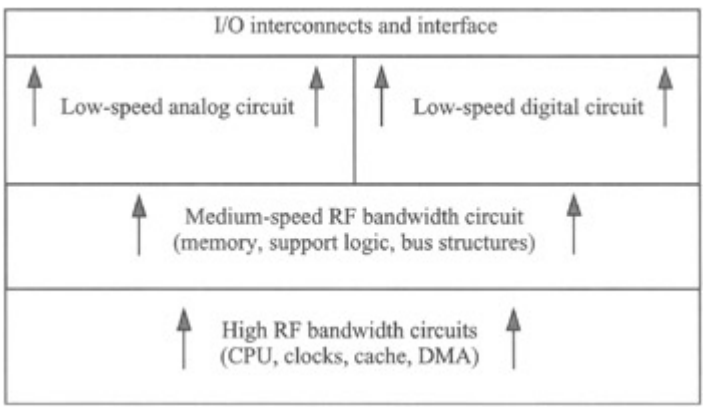

Figure 2.17: Partitioning the PCB in regards to radial migration.

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2.7 COMMON-MODE AND DIFFERENTIAL-MODE CURRENTS

In any circuit, there are both common-mode (CM) and differential-mode (DM) currents, both of which determine the amount of RF energy that is developed and propagated. There is a significant difference between the two. Given a pair of wires or traces and a return path, one or the other mode will exist, usually both. Differential-mode signals carry data or a signal of interest (information). Common mode is a side effect, or a byproduct of differential-mode transmission, and it is most troublesome for EMC compliance. Common-mode and differential-mode currents are illustrated in Fig. 2.18.

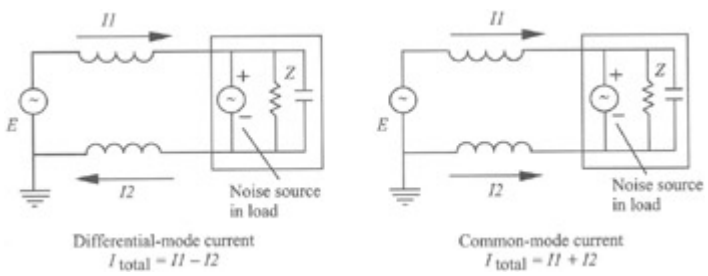

Figure 2.18: Common- and differential-mode current configurations.

2.7.1 Differential-Mode Currents

Radiated emissions from differential-mode (DM) current is the component of RF energy that is present on both the signal and return paths that are opposite to each other. If a 180° phase shift is established precisely, differential-mode current will be canceled. Thus, EMC is assured. In contrast to common-mode (CM) currents, which are usually high-frequency signals, the DM signal may very well not be at RF frequencies. In fact, a DC power line carrying differential-mode DC current (non-RF signal) may be carrying RF common-mode current at the same time.

Differential-mode signals

1. Convey desired information, since most signal traces are a single-ended route (source-to-load). This is the differential mode of data transmission.

2. Cause minimal interference, as RF fields generated oppose each other and cancel out if properly set up, by having the RF return path physically close to the routed trace.

2.7.2 Common-Mode Currents

Common-mode (CM) current is the component of RF energy that is present on both the signal and RF return path, usually in common phase. The measured RF field resulting from common-mode current will be due to the sum of the currents that exist in both the signal trace and the return trace. This summation may be substantial and is the major cause of RF emissions, especially from I/O interconnects. Common-mode current develops through a lack of differential-mode cancellation, or in the presence of poor CM rejection. DM current will exist when there is poor balance in the circuit. This poor cancellation is due to an imbalance between two transmitted signal paths. If the differential signals are not

exactly opposite and in phase to each other, their currents will not cancel out. The portion of the RF field that is not canceled is "common-mode" current. Common-mode effects, however, may also be created as a result of ground bounce and power plane fluctuations caused by components drawing current from a power distribution network.

Common-mode signals are

1. The major source of RF radiated energy.
2. Contain no useful information.

Common mode begins as the result of currents mixing in a shared metallic structure, such as the power and ground planes. Typically, this happens because currents are flowing through undesirable or unintentional return paths. Common-mode currents develop when return currents lose their pairing with their original signal path (e.g., splits or breaks in planes) or when several signal conductors share common areas of the return plane.

In Fig. 2.18, current source, *I1*, represents the flow of current from voltage source, *E*, to load, *Z*. Current flow, *I2*, is current that is observed in the return system, usually identified as an image plane, ground plane, or 0V-reference. The measured radiated electric field of the common-mode current is caused by the summed contribution of both *I1* and *I2*.

A simple analogy that helps explain one way that common-mode energy is developed is to analyze Fig. 2.18 in very simple terms. Assume 1 watt of power is sent from the source to the load. The load dissipates one-half watt of power. This means that current in path *I2* is one-half watt. Under this situation, violation of Ampere's law occurs, which states that the sum of the current in a circuit must equal zero. Visualize now that one-half watt travels toward the source. At the same time, one-half watt travels back from source to load. Mathematically, if we take the limit of the current to zero at any particular point of time, we observe that half of the energy is traveling left, while the other half is traveling right. The summation of these two currents at any particular point of time equals the source current, *I1*; hence Ampere's law is satisfied. This residual one-half watt of power is added to the 1 watt in the source trace. This means that a total of 1-1/2 watts of power is present across the load. This energy is common-mode and is significantly greater than differential-mode current.

With differential-mode currents, the RF energy developed is the difference between *I1* and *I2*. If *I1* = *I2* exactly, there will be no radiation from differential-mode currents that emanate from the circuit (assuming the distance from the point of observation is much larger than the separation between the two current-carrying conductors), and hence, no EMI. This occurs if the distance separation between *I1* and *I2* is electrically small. Design and layout techniques for cancellation of radiated fields emanating from differential-mode currents are easily implemented in a PCB with an image plane or RF return path, such as a ground trace. On the other hand, RF fields created by common-mode currents are harder to suppress.

One design and layout technique to reduce common-mode currents is to decrease the distance spacing between the signal trace and RF current return path, or image plane (power or ground). In most cases, this is not fully possible because the spacing between a signal plane and image plane must be at a specific distance to maintain constant trace impedance of the PCB.

An RF current return path is best achieved with a solid plane for multilayer PCBs or a ground trace for single- and double-sided boards. The RF current in the return path will couple with RF current in the source path (magnetic flux lines traveling in opposite direction to each other). This coupling provides for flux cancellation or minimization, as seen in Fig. 2.19.

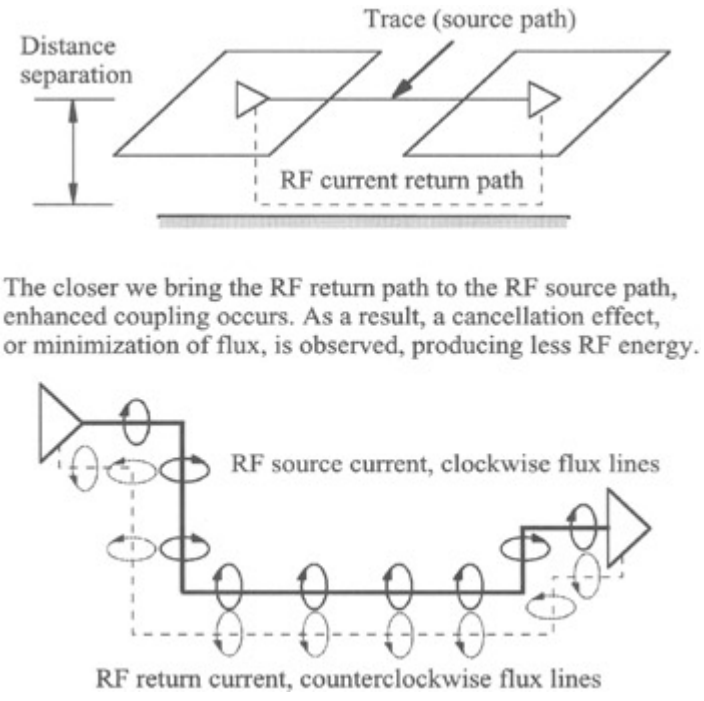
Trace (source path)
Distance
separation
RF current return path
The closer we bring the RF return path to the RF source path,
enhanced coupling occurs. As a result, a cancellation effect,
or minimization of flux, is observed, producing less RF energy.
RF source current, clockwise flux lines
RF return current, counterclockwise flux lines

Figure 2.19: RF current return path and distance spacing.

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2.8 RF CURRENT DENSITY DISTRIBUTION

A 0V-reference or return plane allows RF current to return to its source from a load. This return plane completes the closed-loop circuit requirements for functionality. Current distribution in traces tends to spread out within the return structure, as illustrated in Fig. 2.20. This distribution will exist in both the forward direction and the return path. Current distribution shares a common impedance between trace and plane (or trace-to-trace), which results in mutual coupling due to the current spread. The peak current density lies directly beneath the trace and falls off sharply from each side of the trace into the ground plane structure.

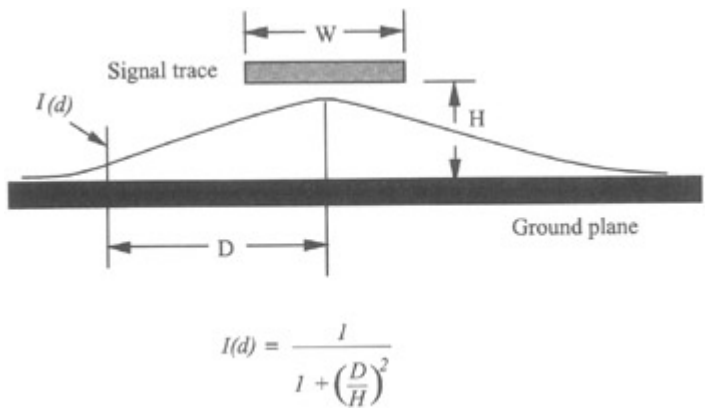

Figure 2.20: Current density distribution from trace to reference plane.

When the distance spacing is far apart between trace and plane, the loop area between the forward and return path increases. This return path increase raises the inductance of the circuit where inductance is proportional to loop area. The current distribution as described in Eq. (2.4) also minimizes the total amount of energy stored in the magnetic field surrounding the signal trace [7].

(2.4) $$I(d) = \frac{I_o}{\pi H} \cdot \frac{1}{1 + \left(\frac{D}{H}\right)^2}$$

Get MathML

where $I_{(d)}$ = signal current density, (A/inch or A/cm)

I_o = total current (A)

H = height of the trace above the ground plane (in. or cm)

D = perpendicular distance from the centerline of the trace (in. or cm)

Depending on the configuration of the topology, RF currents will be developed based on the topologies shown within Fig. 2.21. The distance that the current spreads away from the trace into a reference plane is approximately one transmission line width distance away. For example, if a trace is 0.008 in. (0.002 mm) wide, flux coupling to an adjacent trace will occur if the adjacent trace is less than or equal to 0.008 in. (0.002 mm) away. If the adjacent trace is routed greater than one trace width away,

coupling of RF flux will be minimal. To implement this design technique, the section on the *3-W rule*, located in Section 4.11, details this procedure.

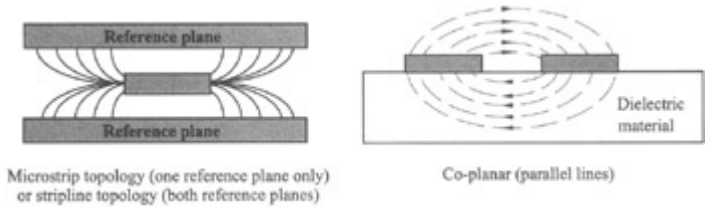
Reference plane
Reference plane
Dielectric material
Microstrip topology (one reference plane only) or stripline topology (both reference planes)
Co-planar (parallel lines)

Figure 2.21: Field distribution for microstrip/stripline and co-planar strips.

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2.9 GROUNDING METHODOLOGIES

Different types of grounding methods are commonly used. The word "ground," by itself is vague and does not represent any specific function within electrical engineering. An adjective must precede the word "ground" to distinguish the type of ground referenced for a particular application. Different types of grounding methodologies include the following. All can be present simultaneously or only one at a time: digital, analog, signal, common, noisy, quiet, isolated, earth, single-point, multipoint, hybrid, chassis, safety, frame, and so on. One grounding topology always forgotten is *RF ground*.

Figures 2.22 through 2.24 illustrate three grounding methods: single-point, multipoint, and hybrid.

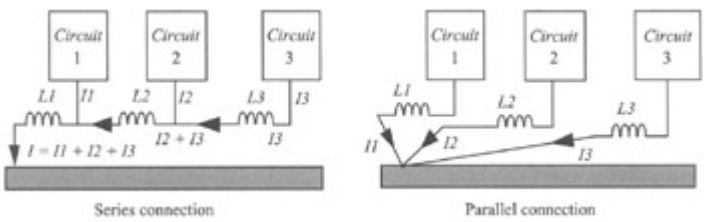

Figure 2.22: Single-point grounding methods. Note: Inappropriate for high-frequency operation.

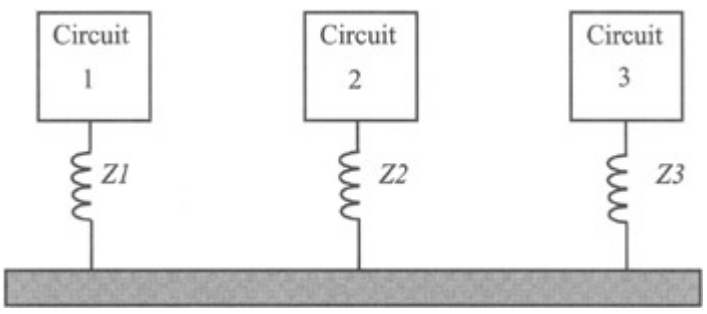

Figure 2.23: Multipoint grounding.

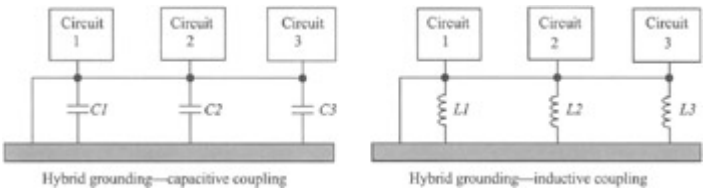

Figure 2.24: Hybrid (frequency selective) grounding configurations.

2.9.1 Single-Point Grounding

Single-point grounding is best when the speed of components, circuits, interconnects, and the like are in the range of 1 MHz or less. At higher frequencies, the inductance of the interconnect will increase the PCB impedance. At still higher frequencies, the impedance of the power planes and interconnect traces become noticeable. These impedances can be very high if the trace lengths coincide with odd multiples of a quarter-wavelength of the edge transitions of components with periodic signals. Not only will these traces and ground conductors have large impedances, they can also act as antennas and radiate RF energy. At frequencies above 1 MHz, a single-point ground generally is not used. However, exceptions do exist if the design engineer recognizes the pitfalls and designs the product using highly specialized and advanced grounding

techniques.

Single-point grounds are usually formed with signal radials and are commonly found in audio circuits, analog instrumentation, and 60-Hz and dc power systems, along with products packaged in plastic enclosures. Although single-point grounding is commonly used for low-frequency products, it is occasionally found in extremely high-frequency circuits and systems.

Use of single-point grounding within a CPU motherboard, or an I/O adapter (daughter card), allows loop currents to be developed between the 0V-reference and chassis housing, if metal is used as chassis ground. Loop currents allow magnetic fields to exist. Magnetic fields create electric fields. Both electric and magnetic fields will develop RF currents that will propagate as either radiated or conducted emissions. It is nearly impossible to implement single-point grounding in personal computers and similar devices because different sub-assemblies and peripherals are grounded directly to the metal chassis in different locations. Induced currents due to electromagnetic fields may couple voltages into a circuit through the mechanism of the transfer, developing loop structures. Multipoint grounding places these loops in regions where they are least likely to cause problems. (RF loop currents can be controlled and directed rather than allowed to transfer energy inadvertently to other circuits and systems susceptible to electromagnetic field disturbance.)

2.9.2 Multipoint Grounding

High-frequency designs generally require use of multiple chassis ground connections. Multipoint grounding minimizes ground impedance present in the power distribution system of the PCB by shunting RF currents from the planes to chassis ground [1]. This lower impedance is caused primarily by the lower inductance characteristic of large, solid copper planes versus that of a small PCB trace or wire. In very high-frequency circuits, the ground leads from components must be kept as short as possible to minimize lead inductance. Lead inductance allows a voltage potential to be developed across the interconnect wire. This voltage potential is one cause of common-mode current generation.

PCB traces add inductance to a circuit or transmission line at approximately 12–20 nH per inch. This variable inductance value is based on two parameters: trace width and thickness. Inductance allows a resonance to occur when both the lumped, distributed capacitance between planes and chassis ground form a tuned resonant circuit. The capacitance value, *C*, is sometimes known, within a specific tolerance range. Inductance, *L*, is determined by knowledge of the impedance of copper planes. The typical value of inductance for a copper plane, 10 × 10 square in. (25.4 × 25.4 square cm), is listed in Table 2.2. The equations for solving an exact value for the impedance of planes is complex and beyond the scope of this book.

Table 2.2: Impedance of a 10 by 10 in. (25.4 × 25.4 cm) Copper Metal Plane

Open table as spreadsheet

Frequency (MHz)	Skin Depth (cm)	Impedance (ohms/square)
1 MHz	6.6×10^{-3}	0.00026
10 MHz	2.1×10^{-3}	0.00082
100 MHz	6.6×10^{-4}	0.0026
1 GHz	2.1×10^{-4}	0.0082

A common architectural concept for many designs is to have a PCB secured to a metal mounting plate or chassis. A resonance is developed between the power and/or ground planes and chassis housing. Figure 2.25 illustrates the capacitance and inductance present between a PCB that is screw secured to a mounting panel or metallic enclosure. Capacitance and inductance will always be present regardless of topology or configuration. Depending on the distance spacing between mounting posts, relative to the self-resonant frequency of the power and ground planes, loop currents will exist. These loop currents are identified as eddy currents and will couple,

either by radiation or conduction to other PCBs located nearby, the chassis housing, internal cables or harnesses, peripheral devices, I/O circuits and connectors, or into free space.

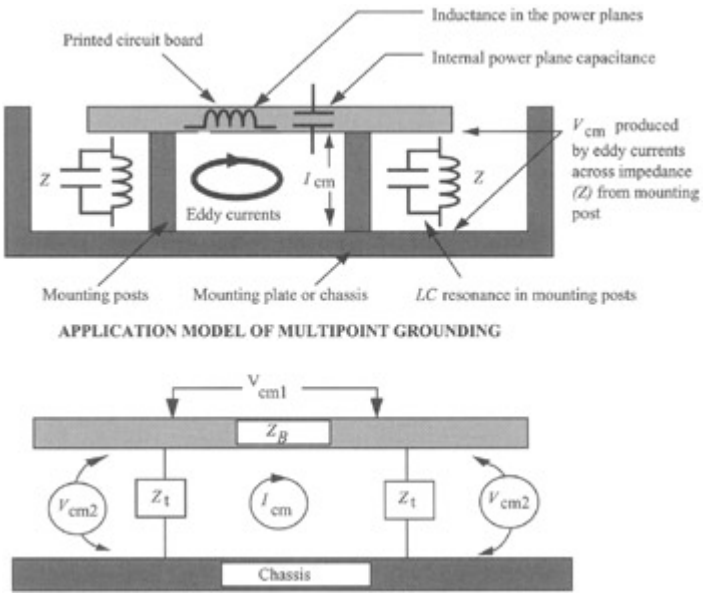

Figure 2.25: Resonance in a multipoint ground to chassis.

In addition to inductance in the planes, physically long traces also act as small antennas when routed microstrip, especially for clock signals and other periodic data pulses. By minimizing trace inductance and removing RF currents or magnetic flux within the transmission line, significant improvement in signal quality and RF suppression will occur. This means coupling RF currents within the transmission line to the 0V-plane or chassis ground.

Digital circuits must be treated as high-frequency circuits. A good low-inductance power distribution network is necessary on any PCB containing many logic devices. The planes internal to the PCB generally provide a lower-inductance return for both power supply and signal currents. This lower inductance allows for creating an enhanced, constant impedance transmission line for signal interconnects. When making ground plane to chassis plane connection, provision must be made for removal of high-frequency RF energy present between the power and ground planes with bypass capacitors. High-frequency RF currents are created by both the resonant circuit of the power distribution network (planes) and their physical relationship to signal traces. It is common to find use of high-quality bypass capacitors, usually 0.1µF in parallel with 0.001 µF at each and every ground connection to remove RF eddy currents, as will be reiterated in Chapter 3.

Chassis grounds must also be frequently connected directly to the ground planes of the PCB to minimize RF voltages and currents that exist between board and chassis. If magnetic loop currents are small (1/20 wavelength of the highest RF generated frequency), RF suppression or flux cancellation or minimization is enhanced [1].

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2.10 GROUND AND SIGNAL LOOPS (EXCLUDING EDDY CURRENTS)

Ground loops are a major contributor to the development and propagation of RF energy. RF current will attempt to return to its source through any available path or medium: components, wire harnesses, power or ground planes, adjacent traces via crosstalk, and so forth. RF current always exists between source and load. This presence is due to the need to have a closed loop for the signal and return path. This loop develops a voltage potential difference between two devices, regardless of whether inductance exists between these points. Inductance in a transmission line causes magnetic coupling of RF current to occur between a source and victim circuit, increasing RF losses in the return path [1].

One of the most important design considerations for incorporating EMI suppression techniques within a PCB is to provide optimal ground or signal return loop control. Engineering analysis must be made for every ground stitch connection (mechanical securement between the PCB ground and chassis ground) to the 0V-reference structure, related to RF return currents developed by RF noisy electrical circuits. To minimize ground voltage potential, high-speed logic and frequency generating components must be located as close as possible to a ground stitch. Placing RF generating components near or adjacent to ground stitch locations will minimize RF current loops, which will develop into the form of eddy currents within the chassis structure. It is imperative that all unwanted RF energy be diverted into the 0V-reference structure.

An example of RF loop currents that could occur in a typical personal computer with adapter cards and single-point grounding is shown in Fig. 2.26. As observed, an excessive return loop area exists between adapter slots and the single-point ground reference. Each loop will radiate a distinct electromagnetic field based on the physical size of the loop. The magnetic field developed within this loop antenna will allow an electromagnetic field to propagate at a frequency that can easily be calculated using simple math [1, 5, 6]. If RF energy is developed from loop antennas present within a PCB layout, containment measures will probably be required. Containment may keep unwanted RF currents from coupling to other systems or circuits in addition to preventing the escape of this energy to the external environment as EMI. Internally generated RF loop currents should always be avoided for both signal functionality and EMI compliance.

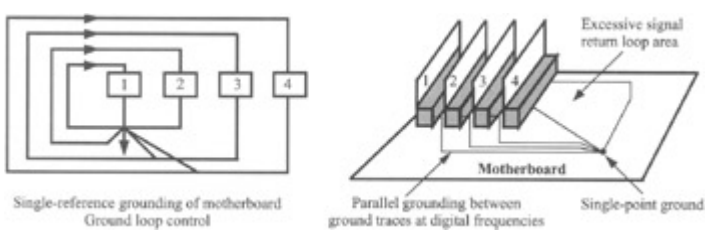

Figure 2.26: Ground loop control.

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Chapter 2 - Printed Circuit Board Basics

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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2.11 ASPECT RATIO—DISTANCE BETWEEN GROUND CONNECTIONS

Aspect ratio is a term commonly used to define the ratio of width to height. The term also refers to the ratio of a longer dimension to a shorter one. With this definition, how does aspect ratio relate to EMC and PCBs? When providing ground stitch connections in a PCB using multipoint grounding to a metallic enclosure, the distance spacing between ground stitch location must be determined in all directions: *x*- and *y*-axis [1].

RF currents that exist within the power and ground plane network tend to couple to components, cables, peripherals, or other electronic items within the assembly. This undesirable coupling may cause improper operation, functional signal degradation, or EMI. When using multipoint grounding to a metal chassis, by providing a third wire ground connection to the AC mains, RF ground loops become a significant design concern. This configuration is typical with personal computers. An example of a single-point ground connection for a personal computer is shown in Fig. 2.26.

Because the edge rates of components are becoming faster, multipoint grounding is becoming a mandatory requirement, especially when I/O interconnect is provided in the design. Once an interconnect cable is attached to a connector, the device at the other end of the interconnect may provide a remote RF path to a third wire AC ground mains connection, if provided for its respective power source. The power source for the load may be completely different from the power source from the driver (e.g., the negative terminal of a battery versus AC). A large RF loop between I/O interconnects can cause undesirable levels of common-mode energy to be observed as either radiated or conducted emissions between the two ends of the cable.

How can we minimize RF loops that may occur within a PCB assembly? The easiest way is to design the PCB with many ground stitch locations to chassis ground, if chassis ground is provided within a multilayer assembly. The question that arises is, How far apart do we make the ground connections from each other, assuming the designer has the option of specifying where the ground stitch location will occur when implementing this design technique?

The distance spacing between ground stitch locations should not exceed λ/20 of the highest frequency, or harmonic of concern, not just the primary frequency of interest. If many high-bandwidth components are used, multiple ground stitch locations are typically required. If the unit is a slow edge rate device, connection to chassis ground may be minimized, or distance spacing between ground locations may be increased. This separation should be related not to the clock rate but to the highest harmonic frequency of the circuit.

The reason this distance spacing is selected is due to characteristic features of dipole antennas. An efficient antenna can exist with dimensions down to λ/20 of the highest generated frequency, or harmonic. A finite impedance exists within the ground structure, which is one side of a dipole antenna. The signal trace contains RF energy, which is the driven element of the dipole. Thus, between two locations on the PCB, an antenna structure is developed. The concept of multi-point grounding is to minimize the dipole effect created between signal traces and a return path. The

smaller we make the distance spacing between two locations, the higher the resonant frequency of the antenna, resulting in less EMI being developed internal to the PCB assembly.

For example, λ/20 of a 64-MHz oscillator is 9.2 in. (23.4 cm). If the straight-line distance between two ground stitch connections to a 0V-reference in either the *x*- or *y*-axis is greater than 9.2 in. (23.4 cm), a potential efficient RF loop exists. This loop could be the source of RF energy propagation, which could cause noncompliance with international EMI emission limits. Unless other design techniques are implemented, suppression of RF currents caused by poor loop control is not possible and containment measures, such as sheet metal must be implemented. Sheet metal is an expensive cost that might not work for RF containment. Aspect ratio is illustrated in Fig. 2.27, where the distance spacing between ground locations is less than λ/20 in all directions.

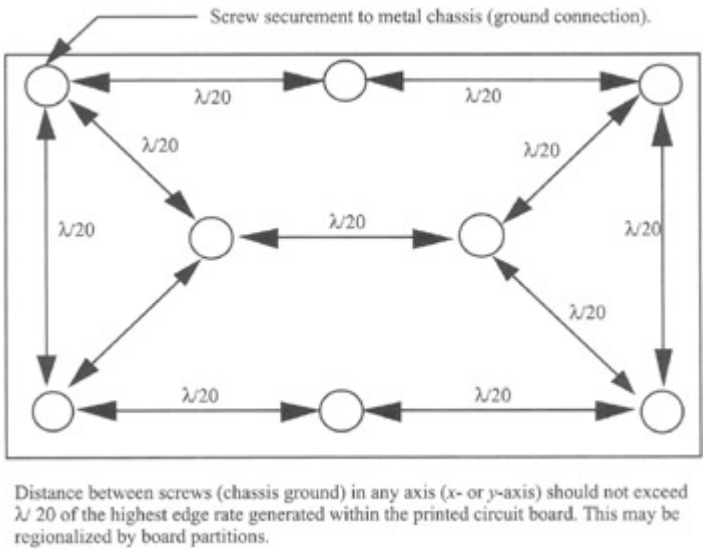
Screw securement to metal chassis (ground connection).
λ/20
λ/20
λ/20
λ/20
λ/20
λ/20
λ/20
λ/20
λ/20
Distance between screws (chassis ground) in any axis (x- or y-axis) should not exceed λ/ 20 of the highest edge rate generated within the printed circuit board. This may be regionalized by board partitions.

Figure 2.27: Example of aspect ratio.

This chapter deals with the basics of EMC related to printed circuit boards. Implementation of layout concepts has not yet been discussed. Since the subject of aspect ratio using a multiground methodology has been covered, we now consider a design technique for use on a PCB with multipoint grounding.

With many chassis ground connections, how does one incorporate a cost-effective technique for making numerous ground points without use of screws for mechanical securement? Alternative techniques and material are available, with an overall cost less than the screw-secured connection, once labor costs are factored in. An example of a creative technique for providing numerous ground stitch locations, using only several screws for mechanical securement, is shown in Fig. 2.28. The material illustrated is an EMI-conducted cloth gasket on a neoprene sponge core. Other material may be used, such as beryllium copper fingers. Many manufacturers provide conductive material in any size, shape, and configuration imaginable. This technique has been applied numerous times with extreme success.

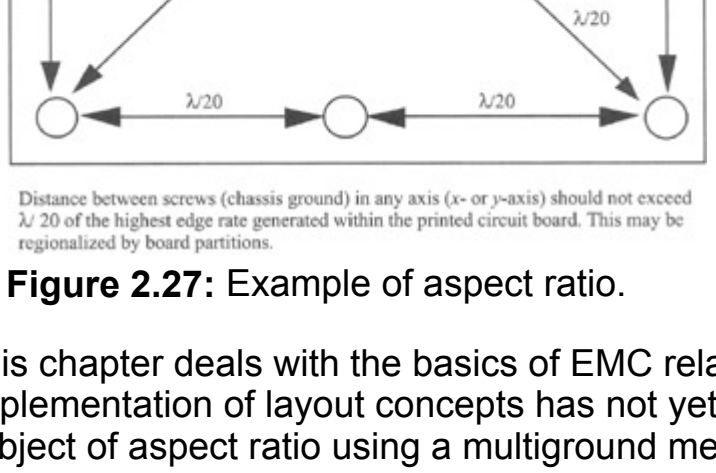

Figure 2.28: Creative technique for providing multipoint ground connection.

Use of this design implementation *must* be made long before component placement is finalized on the PCB and before mechanical design of the enclosure. What we want to achieve, for example, is 20 or more ground stitch points from the PCB to the chassis, in addition to the required screw connections. Between the PCB and metal mounting plate, or enclosure housing, a physical distance is present. This distance is due to the use of

pem-studs or equivalent securement provided in the chassis enclosure. The height of the PCB above the chassis housing is typically 0.25 in. (0.64 cm). Within this spacing, placement of conductive gasket occurs using a mylar sheet of plastic as an alignment and support bracket. Holes are punched into this mylar sheet. The gasket, in the shape of an I-beam 0.125 in. (3.2 mm) square is inserted into each punched hole. The mylar sheet is then located over existing pre-specified screw-secured mechanical locations. These locations provide securement of the PCB to the mounting plate for structural requirements. These screw locations may be predefined by the architecture of the product. Relocation of these screw securement points may not be possible. For personal computers, screw locations are fixed for compatibility between vendors.

After component placement, before routing, multipoint ground locations should be identified. A plated through-hole pattern is provided on the bottom layer of the PCB. However, an actual through-hole is not incorporated. On the bottom of the PCB, a non-solder mask circular pattern is made, as if this location were an actual through-hole pad for screw securement. The diameter of this pattern on the bottom of the PCB must be very large, approximately 0.25 to 0.50 in. (0.64 to 1.28 cm)! A large pattern is needed to accommodate for tolerance connection between the gasket and PCB. With a sponge core, the conductive material will spread out in all directions. The oversize pattern of the ground point accommodates for the slop in the mechanical connection and allows for optimal bonding between the gasket and PCB. This large pattern also prevents discrete or active components near the ground location from being shorted out by the conductive material. Multiple vias connections from the ground plane internal to this multilayer PCB must be provided to the ground pad, without disrupting the ability of the autorouter to perform its task. The height of the gasket must be greater than the physical dimension of the standoff. This additional height requirement permits compression of the gasket once the PCB is installed and screw-secured.

Once all ground connections are determined and the PCB is installed into the enclosure, screws are provided to mechanically secure the PCB to the chassis. The PCB presses down on the conductive gasket. The gasket will spread out on both the top and bottom side of the mylar sheet, thus assuring a low-impedance bond connection between PCB and chassis. If a different PCB layout is required with this same chassis, but component placement and ground point requirements become different, hole locations in the mylar sheet can be redefined, thus preventing a redesign of the enclosure. This is where cost savings become significant. It is cheaper to punch holes in a mylar sheet than to retool a sheet metal chassis or re-layout a PCB.

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2.12 IMAGE PLANES

An image plane is a layer of copper or similar conductive internal to a PCB. This layer may be identified as a voltage plane, ground plane, or 0V-reference plane physically adjacent to a circuit or signal routing layer. Image planes provide a low-impedance path for RF currents to return to their source (flux cancellation or minimization). A complete return path must be present for the circuit to function. This return path is for both signal and RF current. With an optimal RF return path, the development of EMI is reduced. The term "image plane" was popularized by Ref. [8] and is now used as industry standard terminology.

RF currents must return to their source one way or another. This path may be a mirror image of its original trace route or through another trace located in the near vicinity (crosstalk). This return path may be a power plane, ground plane, or free space. RF currents will capacitively or inductively couple themselves to any transmission line that has a lower impedance than the previously defined path.

An image plane reduces ground noise voltage in addition to allowing RF currents to return to their source (mirror image) in a tightly coupled manner. Coupling approaches 100%, but can never achieve this value, because a physical distance separation must be maintained between layers within a PCB assembly. Tight coupling between the signal and return path provides for enhanced flux cancellation or minimization between the two paths, which is another reason for using a solid return plane without splits, breaks, or oversized through-holes. An example of how an image plane appears to a signal trace is detailed in Fig. 2.29.

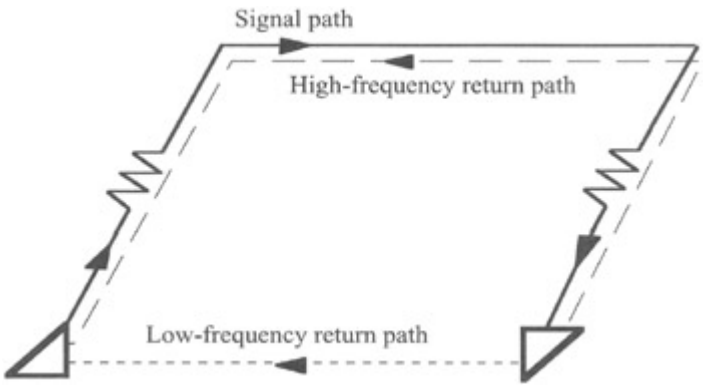

Figure 2.29: Image plane concept.

Regarding image plane theory, the material presented herein is based on a finite-sized plane. All PCBs are finite. Image planes cannot be relied on to reduce or remove RF currents that exist on I/O cables and interconnects. This restriction is owing to approximating finitesized conductive planes when dealing with signals that travel off the PCB. When I/O interconnects are provided, the dimensions of the source and load impedance are the important parameters to remember [9].

Image planes work as well as they do for the following reasons:

> Multilayer boards provide superior signal quality and EMC performance, since signal impedance control is enhanced using either stripline or microstrip topology. The distribution impedance of the power and ground plane structure must be dramatically reduced. Power and ground planes contain RF spectral current surges caused by logic crossover, momentary shorts, and

capacitive loading on signals with wide buses. Central to the issue of microstrip or stripline routing is understanding flux cancellation or flux minimization that minimizes or controls inductance within any transmission line. Various logic devices may be quite asymmetrical in their pull-up/pull-down current ratios.

Asymmetrical current draw in a PCB causes an unbalanced situation to exist. This imbalance relates to flux cancellation or minimization. Magnetic flux will travel through return current paths that are present within the ground or power plane, or both, depending on stackup and component technology. Generally, ground return for TTL is preferred. For ECL, positive return is used. This is why ECL generally runs on -5.2V, with the more positive line at ground potential. CMOS is more or less symmetrical so that, on the average, little difference exists between the ground and voltage planes. One must look at the entire equivalent circuit before making a judgment.

To briefly restate this important concept related to flux cancellation or minimization, it is noted that not all components behave the same way on a PCB related to their pull-up/pull-down current ratios. For example, some devices have 15-mA pull-up/35 mA pull-down. Other devices may have a 25-mA pull-up/pull-down ratio (or 50%). When many components are provided, asymmetrical power consumption will occur when all devices switch simultaneously. This asymmetrical condition creates an imbalance in the power and ground plane structure. The fundamental concept of board-level suppression lies in flux cancellation or minimization of RF currents within the board related to traces, components, and circuits referenced to 0V. Power planes, owing to flux phase shift from many components switching asymmetrically, may not perform as well for flux cancellation as ground planes because of the situation noted above. Consequently, optimal performance may be achieved when traces are routed adjacent to 0V-reference planes, and not adjacent to power planes.

If three internal routing layers are physically adjacent in a multilayer stackup assignment, the middle layer (e.g., the one not immediately adjacent to an image plane) will couple its RF currents (energy) to the other two adjacent signal planes. An example of this poor stackup requirement is detailed in Fig. 2.30. This poor assignment will result in undesired RF energy transfer through both mutual inductive and capacitive coupling to the other signal planes. This coupling can cause significant crosstalk to occur. Flux cancellation performance is enhanced when all signal routing layers are adjacent to a 0V-reference or ground plane, and not adjacent to a power plane. The reason for this statement is that the power distribution network generally contains more switching energy than the 0V-reference or return network. The switching energy from digital devices sometimes transfers or couples RF energy to other functional areas, whereas the 0V-reference or return structure is generally held at ground potential, which is by nature more stable than power. The exception to this requirement occurs when excessive ground bounce, or board-induced noise voltage is present, causing common-mode energy to be developed. By referencing a reference layer to ground potential, circuits and cable interconnects should not be modulated by switching currents that may be present in the power distribution network.

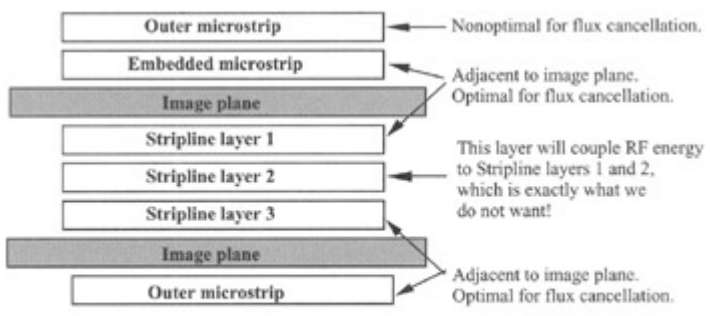
Outer microstrip
Nonoptimal for flux cancellation.
Embedded microstrip
Adjacent to image plane.
Optimal for flux cancellation.
Image plane
Stripline layer 1
This layer will couple RF energy
to Stripline layers 1 and 2,
which is exactly what we
do not want!
Stripline layer 2
Stripline layer 3
Image plane
Adjacent to image plane.
Optimal for flux cancellation.
Outer microstrip
Eight-layer PCB with six routing and two reference planes (DO NOT USE)!
Note: The image planes may be at either ground or power potential.

Figure 2.30: Poor stackup assignment—no image plane for middle stripline layer.

For image planes to be effective, *no traces can be located within this solid planar structure*. Exceptions are possible when a moat, isolation, or absence of copper occurs. If a signal route, or a power trace (e.g., +12 V),

is located within a solid +5V plane, this +5V plane becomes fragmented. Provisions have now been made for a ground or signal return loop to be present for signal traces routed on the adjacent layer across this violation. This loop area occurs because RF return currents cannot seek a straight-line path back to its source. Split planes can no longer function as a low-impedance, solid return path for RF currents to complete the trip in an efficient manner for optimal flux cancellation.

Figure 2.31 illustrates a violation of image plane requirements. An image plane that is not a solid structure cannot function as an optimal return path. If an optimal return path is not present, common-mode RF currents will be developed owing to loss of balance differentially in the loop circuit. This loss across the plane segmentations will produce RF fields.

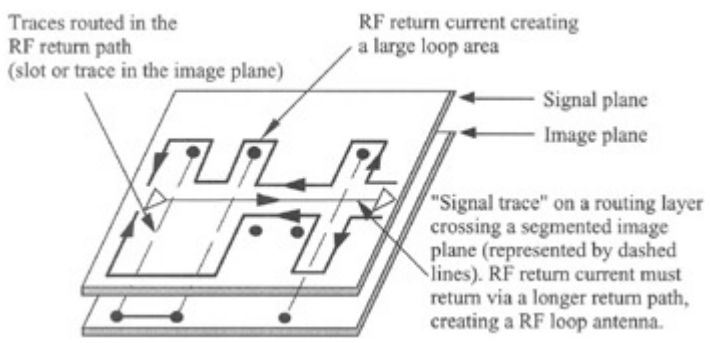
Traces routed in the
RF return path
(slot or trace in the image plane)
RF return current creating
a large loop area
Signal plane
Image plane
"Signal trace" on a routing layer
crossing a segmented image
plane (represented by dashed
lines). RF return current must
return via a longer return path,
creating a RF loop antenna.

Figure 2.31: Image plane violation with traces.

Vias placed in an image plane do not degrade the imaging capabilities, except where continuous slots are provided, as discussed in the next section. Vias do, however, affect other functional parameters in a PCB layout. These functional parameters include

- Reducing interplanar capacitance; degrading decoupling efficiency.
- Preventing RF return currents from jumping between routing or image planes.
- Adding more inductance and capacitance to a trace route.
- May create an impedance discontinuity within the transmission line structure.

Figure 2.32 illustrates the effect of loop areas when vias are incorporated within image planes. Excessive through-hole pin clearance, or poor pin assignment strategies during connector assignment, can lead to an excessive loop area for return currents, exacerbating the development of common-mode RF energy. When signal and return traces are separated, the loop area can become significant, radiating RF energy. It is important for the design engineer to know and understand where the return signal path is and to guarantee that the loop area defined is as small as possible.

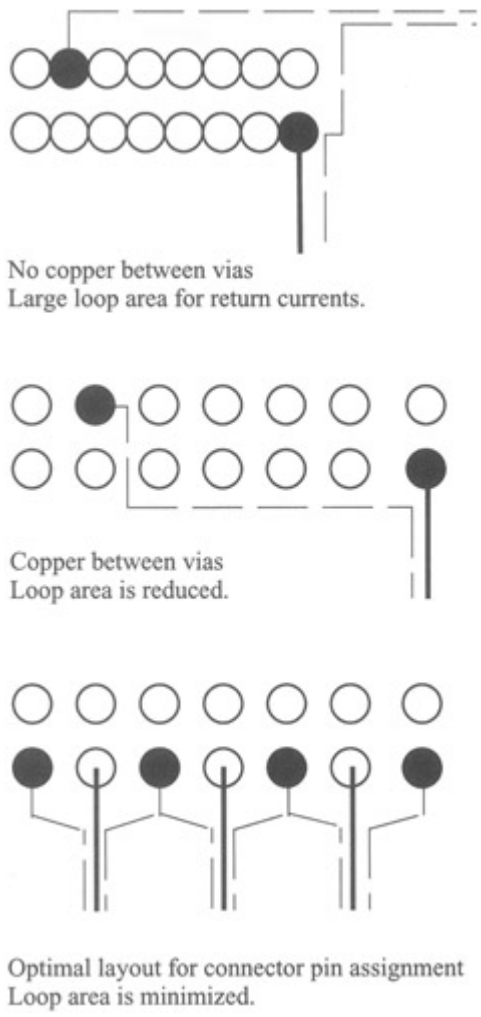
No copper between vias
Large loop area for return currents.
Copper between vias
Loop area is reduced.
Optimal layout for connector pin assignment
Loop area is minimized.

Figure 2.32: Loop areas with vias in the image plane.

Figure 2.32 illustrates three configurations. In the top illustration, there is no copper between the vias for the return trace to allow RF current to travel back to its source. The return current must travel around the connector, or the through-hole component to the ground pin, causing a potential significant loop area. This loop area may result in unacceptable emission levels of RF energy. An improved method of manufacturing the board, the middle illustration, allows copper to be present between the vias. This configuration enhances the return current's ability to travel through the via. In the bottom illustration, an optimal method of assigning connector pins exists, thus allowing for enhanced return of RF current. For further discussion of this item, see both the next section and Chapter 7.

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2.13 SLOTS WITHIN AN IMAGE PLANE

A concern associated with image plane discontinuity is use of through-hole components. An excessive number of through-holes within a power or ground plane structure creates a situation identified as the Swiss cheese syndrome [10]. The copper between through-hole pins is reduced because many holes overlap each other, leaving large areas of discontinuity. This occurs because during the manufacturing process, oversized through-holes are drilled. Oversized holes are drilled because they reduce the cost of manufacturing by allowing a greater tolerance for the manufacturer of the bare board assembly. An example of oversized drilled holes is provided in Fig. 2.33. The return current flows in the image plane adjacent to the signal route. The RF return current cannot mirror image to the signal trace on the adjacent layer due to this discontinuity. As seen in the figure, return currents in the ground plane must travel around the through-hole slots. This extra RF return path length creates a loop antenna, developing a magnetic field between the signal trace and the return path. Additional inductance in the return path also means less flux cancellation. For through-hole components that have copper between pins (nonoversized holes), reduction of signal and return current of magnetic flux is achieved. This flux reduction is due to less inductance in the signal return path owing to the solid image plane.

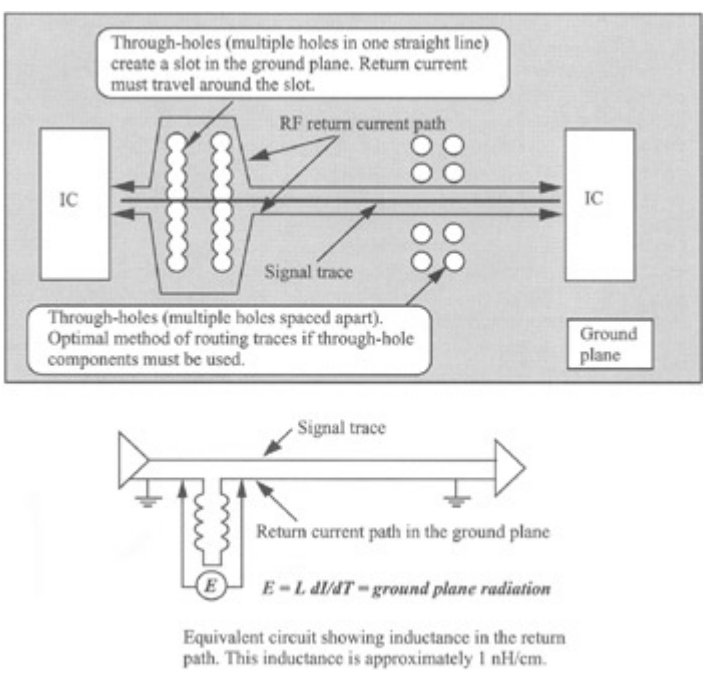
Through-holes (multiple holes in one straight line) create a slot in the ground plane. Return current must travel around the slot.
RF return current path
IC
IC
Signal trace
Through-holes (multiple holes spaced apart). Optimal method of routing traces if through-hole components must be used.
Ground plane
Signal trace
Return current path in the ground plane
E
E = L dI/dT = ground plane radiation
Equivalent circuit showing inductance in the return path. This inductance is approximately 1 nH/cm.

Figure 2.33: Ground loops when using through-hole components (slots in planes).

If the signal trace is routed "around" through-hole discontinuities (the left-hand side of Fig. 2.33), a constant RF return path cannot be maintained along the entire signal route. The opposite is true for the right-hand side of Fig. 2.33. For here, a continuous image plane is present; hence, there is not a short, direct-line RF return path. Problems can however arise when a signal trace travels through the middle of slotted holes. When routing traces between through-hole components, provision must be made for at least three times the width of the trace between the signal trace and though-hole location. This distance spacing ensures that optimal flux cancellation will occur, as magnetic flux must couple to the routed trace, not into the component read.

Generally, slots in a PCB with oversized or overlapping holes will not cause RF problems for the majority of signal traces routed between through-hole

device leads. This observation is valid for traces that do not carry high levels of RF energy or static level signals, not clock or period traces. For high-speed, high-threat signals, alternative methods of routing traces between through-hole component vias must be devised. For applications in which a trace must traverse across a slot or partition within the PCB assembly, Fig. 2.34 provides a simple design technique. This design technique guarantees that RF current has the ability to achieve a direct-line return path back to the source.

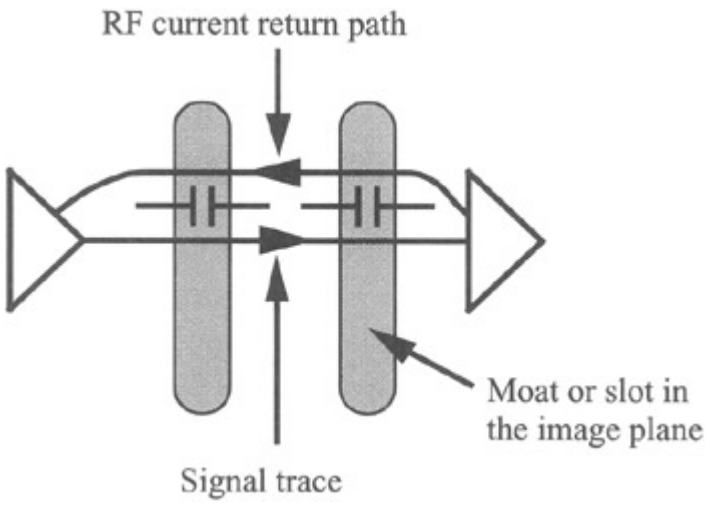

Figure 2.34: Crossing a slot to allow RF return current to pass.

Capacitors provide an AC shunt, or path, for RF currents to traverse across a moat or slot. The DC signal level is unaffected by this capacitor. A performance improvement of up to 20 dB has been observed during functional testing. The capacitor must be chosen for optimal performance based on the self-resonant frequency of the component trace signal.

A continuous image plane is still the best choice when splits or moats are provided. This is especially true when both analog and digital circuitry is provided. Attempting to isolate analog and digital ground planes sometimes provides enhanced performance by not allowing RF energy from one functional area to corrupt other functional areas. Problems develop when a trace must cross this moat or there is an absence of copper area. The trace will see a large impedance discontinuity. If several similar signals cross the same boundary and simultaneous switching occurs, a significant amount of common-mode energy may be developed, especially when all signals attempt to switch logic state at the same time, in the same direction: logic HIGH or LOW. If several bypass capacitors are provided across the boundary violation to eliminate the problem, as shown in Fig. 2.34, a continuous RF return path should have been provided to begin with.

In addition to reducing ground-noise voltage between source and load, image planes prevent ground loops from developing. This is because RF return current tends to couple to its source trace without having to find another path home. Loop control is maintained and minimized. Placement of an image plane adjacent to each signal plane removes common-mode RF currents created by signal traces. Image planes carry high levels of RF currents that must be sourced to ground potential. To help remove excess RF energy, all 0V-reference and chassis planes must be connected to chassis ground by a low-impedance ground stitch connection [1, 11].

One concern relating to image planes centers on the issue of skin effect. *Skin effect* refers to high-frequency current flow that resides in the first skin depth of the material. Current does not, and cannot, significantly flow in the center of traces, wires, or planes, and it is predominantly observed on the outer surface of conductive media. Different materials have different skin depth values. The skin depth of copper, for example, is extremely shallow above 30 MHz. Typically, this is observed, for example, as 0.0000066 in. (0.0017 mm) at 100 MHz. RF current therefore cannot penetrate a 1-oz. copper layer that is beyond 0.0014 in. (0.036 mm) thick. As a result, both common-mode and differential-mode currents flow only on the top (skin) layer of the plane. No significant current flows internal to the image plane or on its bottom. Placing a second image plane adjacent to a primary reference plane would not provide additional EMI reduction. If the second reference plane is at voltage potential (the primary plane at ground potential), a decoupling capacitor is created between these two planes. These two planes can now be used for both decoupling and imaging [1].

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2.14 FUNCTIONAL PARTITIONING

Proper placement of components for optimal functionality and EMC suppression is important in any layout. Most designs incorporate functional subsections or areas by logical function. Grouping functional areas minimizes signal trace length, routing, and creation of antennas. Proper component placement also makes trace routing easier, thus enhancing signal integrity. Figure 2.35 illustrates functional grouping of subsections, or areas, on a complex motherboard design.

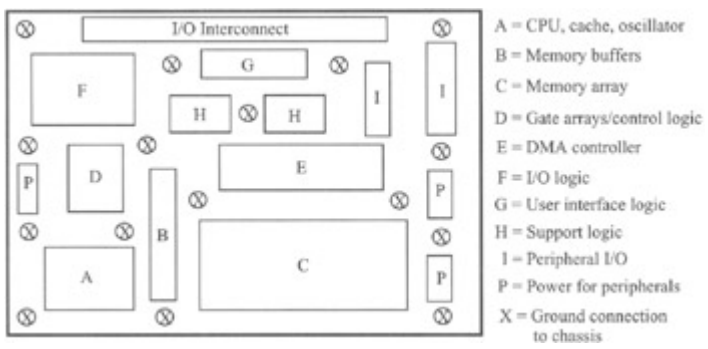

Figure 2.35: Functional grouping and multipoint grounding implementation.

Extensive use of chassis ground stitch connections is illustrated in the figure. One method of implementing numerous ground connections was detailed in Section 2.11 (Fig. 2.28). High-frequency, high-technology designs require new methodologies for bonding ground planes to chassis ground. Multipoint grounding effectively partitions common-mode currents that emanate between various sections in the design. This partitioning also keeps RF currents coupling from one section into other sections. Products with clocks above 50 MHz generally require frequent ground stitch connections to chassis ground. This grounding minimizes the effects of common-mode currents and ground loops present between the functional sections. At least four ground points surround each section. These ground points illustrate best-case implementation of maintaining an optimal aspect ratio around functional sections, although this ratio is not always economically feasible.

Note in Fig. 2.35 that a chassis bond connection, screw or equivalent, is located on both ends of the DC power connector (Item P) used for powering external peripheral devices. RF noise generated by the peripheral power subsystem must be AC shunted to chassis ground using decoupling capacitors. Decoupling capacitors reduce the coupling of power-supply-generated RF currents into both the signal and data lines. Shunting of unwanted RF currents on the power connector also optimizes signal integrity for data transfer between the motherboard and external peripheral devices, in addition to reducing both radiated and conducted emissions [1, 11].

Most PCBs consist of functional subsections or areas. For example, a typical personal computer contains the following: CPU, memory, ASICs, bus interface, system controllers, PCI bus, SCSI bus, universal serial bus (USB), peripheral interface (fixed and floppy disk drives), video, audio, and other components. Associated with each area are various bandwidths of RF energy. Digital components generate RF energy throughout the frequency spectrum. The higher the frequency component of the signal (faster edge rate), the greater the bandwidth of RF spectral energy generated from both the frequency of operation along with the time-variant

edges of digital signal transitions. Clock signals are the greatest contributor to the development of RF energy because clock signals are periodic, approximately 50% duty cycle.

To prevent RF coupling between different bandwidth areas, functional partitioning is required. *Partitioning*, another word for physical separation between functional sections, is product specific and may be achieved using multiple PCBs, isolation between assemblies, and various topology layouts, or incorporating other creative means.

Proper partitioning also allows for optimal signal functionality and ease of routing traces while minimizing overall trace lengths. Partitioning permits smaller RF loop areas to exist, optimizing signal quality. The design engineer must specify to the PCB designer which components are associated with each functional subsection. The information provided by component manufacturers and design engineers can be used to optimize component placement prior to routing any traces.

Functional partitioning can also be thought of as the process of separating one functional area from another functional area for the purpose of maintaining isolation between dissimilar circuits (Fig. 2.36). Functional partitioning of the power and ground planes in an I/O area prevents RF currents in one section of the PCB from entering another area. What we want to achieve is to keep electromagnetic fields associated with a particular subsection to the area that requires this energy. Transference of electromagnetic energy from a clock distribution area is not desirable for I/O circuits or interconnects. The distance separation between processor and I/O must be well decoupled, RF-wise, as a finite voltage potential difference occurs. Whenever a voltage potential difference exists, common-mode energy develops between the two zones. Once we connect a cable to the PCB, common-mode energy is transferred from the power distribution system and signal trace onto the attached antenna. I/O interconnects will radiate common-mode and/or differential-mode RF energy. Keeping unwanted RF energy from high-bandwidth areas from entering the I/O section (low-bandwidth areas) or other functional areas is the ultimate design objective during layout and routing.

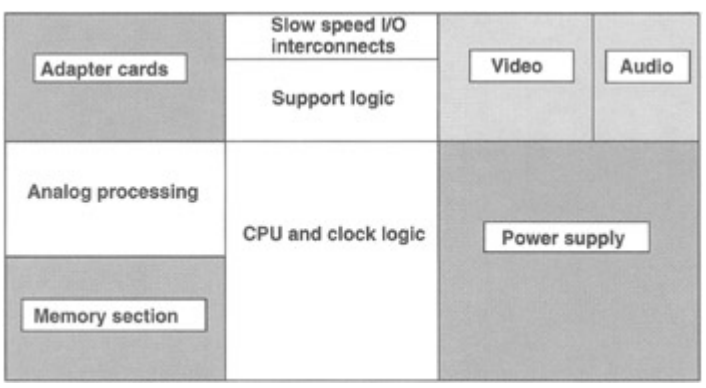

Figure 2.36: Functional partitioning.

Functional partitioning presents two concerns; these concerns deal with both conductive and radiated RF energy. Conductive RF energy travels between functional areas through signal traces and the power distribution network, whereas radiated energy is transferred through free space.

If it is impossible to develop an optimal partitioned layout, another technique to control emissions and enhance immunity of the PCB is to provide an overall shield partition around the section developing the undesired RF energy. Even with a metal shield partition, it may be impossible to ensure the integrity of the shield, while permitting proper operation of the circuits. The built-in apertures and slots associated with a shield preclude effective RF attenuation for radiated energy at high frequencies, generally above 800 MHz.

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2.15 CRITICAL FREQUENCIES (λ/20)

Throughout this book, reference is made to critical frequencies or high-threat clock and periodic signal traces that have a wavelength greater than λ/20. The following equations show how to calculate the wavelength of a signal and the corresponding critical frequency. A summary of miscellaneous frequencies and their respective wavelength distance is presented in Table 2.3 based on these equations.

Table 2.3: λ/20 Wavelength at Various Frequencies

Open table as spreadsheet

Frequency	λ Distance	λ/20 Wavelength Distance
10 MHz	30 m (32.8 ft)	1.5 m (5 ft)
27 MHz	11.1 m (36.4 ft)	0.56 m (1.8 ft)
35 MHz	8.57 m (28.1 ft)	0.43 m (1.4 ft)
50 MHz	6 m (19.7 ft)	0.3 m (12 in.)
80 MHz	3.75 m (12.3 ft)	0.19 m (7.52 in.)
100 MHz	3 m (9.8 ft)	0.15 m (6 in.)
160 MHz	1.88 m (6.15 ft)	9.4 cm (3.7 in.)
200 MHz	1.5 m (4.9 ft)	7.5 cm (3 in.)
400 MHz	75 cm (2.5 ft)	3.75 cm (1.5 in.)
600 MHz	50 cm (1.6 ft	2.5 cm (1.0 in.)
1000 MHz	30 cm (0.98 ft)	1.5 cm (0.6 in.)

(2.5)
$$f(MHz) = \frac{300}{\lambda(m)} = \frac{984}{\lambda(ft)}$$

$$\lambda(m) = \frac{300}{f(MHz)}$$

$$\lambda(ft) = \frac{984}{f(MHz)}$$

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2.16 LOGIC FAMILIES

When selecting a component for a particular application, design engineers are generally interested only in functionality, operating speed, and propagation delay of the internal logic gates as published by the manufacturer. Consideration of electromagnetic effects is seldom considered.

As components become faster (decrease in internal propagation delay), an increase in RF current, crosstalk, and ringing will occur, based on the inverse relationship between speed and EMI. A device is generally chosen based on the propagation time from input to output, along with the setup time of the input signal. Almost all components have internal logic that operate at a faster edge rate than the propagation delay required for functionality. Consequently, slower logic families (internal gates) are preferred. Figure 2.37 illustrates the relationship between the internal switching speed of a basic inverter gate compared to propagation delay.

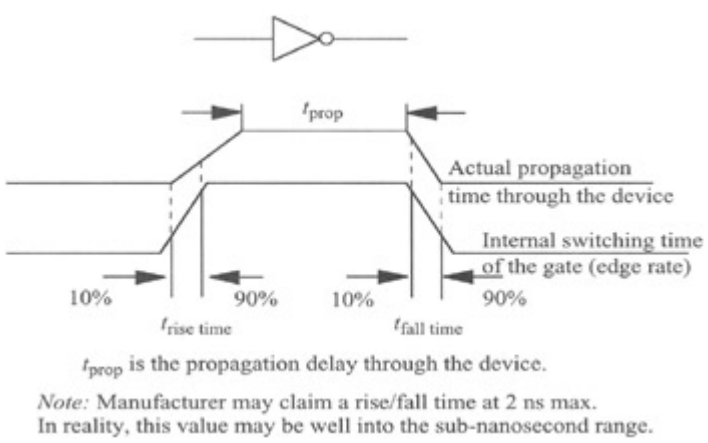
t_{prop}
Actual propagation time through the device
Internal switching time of the gate (edge rate)
10%
90%
10%
90%
$t_{rise\ time}$
$t_{fall\ time}$
t_{prop} is the propagation delay through the device.
Note: Manufacturer may claim a rise/fall time at 2 ns max.
In reality, this value may be well into the sub-nanosecond range.

Figure 2.37: Output switching time versus propagation delay.

Various logic families are available with different design features. These features vary between CMOS, TTL, and ECL, to name a few. Some of these features include input power consumption, package outline, speed-power combinations, voltage swing level, and edge transition rates. Certain logic devices are available with clock skew circuitry to control the internal edge transitions of the internal logic gates, while maintaining accurate propagation delay through the component.

One extremely important device parameter that device manufacturers do not usually specify in data sheets is *peak inrush surge current into the device operating under maximum capacitive load*. Peak surges are the result of logic crossover currents, device capacitive overheads, individual trace capacitance, and device junctions. Input surge current may exhibit levels that are many multiples of the actual signal currents driven, and it can be as much as ten times quiescent levels!

Crossover currents are developed when digital devices change logic state. For a finite time period, the voltage to the component is shorted to ground when the output transistors switch. This short is usually in the low picosecond range and is generally too fast to be measured with most instrumentation. This spike is sometimes observed on a spectrum analyzer as a walking transition that is difficult to trigger on.

Device capacitive overhead refers to the total amount of current that a component must source to all output pins that drive other devices. When

we send an electromagnetic field down a transmission line, current is required to charge the load. This load will always be capacitive. Current must come from somewhere. This somewhere is the power distribution system *through* the component. Thus, if the source sends 25 mA to a load, this 25 mA is added to the quiescent or steady-state current of the device. This surge lasts a brief period, whereas the quiescent is constant. If there are ten drivers, up to 250 mA of current may be consumed from the power distribution network through the component during the transition switching state, *in addition* to quiescent current. Few engineers recognize this fact.

2.16.1 Edge Rate Transitions

Selection of the slowest possible logic family, while maintaining adequate timing margins, minimizes EMI effects and enhances signal integrity. Devices with edge times (*tr*) greater than 5 ns, if possible, should be used for applications when the timing requirement of functionality allows. Use of standard and low-power Schottky TTL (e.g., 74LS series) is becoming less common in today's marketplace, and they are becoming more difficult to purchase. Design techniques presented herein are usually not required when using slower-speed logic families. However, today's high-speed, high-technology products find use of extremely fast edge transition logic that is significantly less than 2 ns, or in the sub-nanosecond range, such as the 74ACT and 74F series. A 74HCT could be provisionally adequate for replacement of a 74ACT device for some applications, with the added benefit of less RF energy created. As a general consideration, one should not use faster devices than the functional timing diagram of the circuit actually demands, which may be *impossible* to do with the availability of components and marketing requirements.

Fast edge transitions cause a proportional increase in problems related to return currents, crosstalk, ringing, and reflections. This is because logic families have edge rates that are always faster than the propagation delay inherent in the device. No two logic families are the same. The same components (form, fit, and function compatible) from different manufacturers differ in construction and manufacturing processes, including edge transition times. Edge rate is defined as the rate of voltage or current change per unit time (volts/ns or amperes/ns).

When selecting a logic family, manufacturers will specify in their data books the "maximum" edge rate, t_{rmax}, of the clock and I/O pins. Generally, this specification is usually 2–5 ns maximum. It is observed that, typically, the "minimum" edge rate, t_{rmin}, is not provided. A device with a 2-ns maximum edge rate specification may in reality have a 0.5 to 1.0-ns edge rate device. The greatest contributor to RF energy is the edge rate transition, not actual operating frequency! A 5-MHz oscillator driving a 74F04 (with a 1-ns edge) will generate larger amounts of RF spectral energy than a 50-MHz oscillator driving a 74ALS04 (with a 4-ns edge). **This one component specification is the most frequently overlooked and forgotten parameter in PCB design; however, this is a design engineer's most critical concern to ensure an EMI compliant product.** This is a frequency domain issue (EMI) and not a time domain (signal integrity) issue.

The frequently heard statement, "Use the slowest logic family possible," goes back to the component manufacturers' failure to specify or publish this minimum edge rate parameter in their data books. The edge rates of digital components are the source of most RF energy developed within a PCB. Table 2.4 illustrates published, not actual edge rate transition levels.

Table 2.4: Sample Chart of Logic Families, Illustrating Spectral Bandwidth of RF Energy

➪ Open table as spreadsheet

Logic Family	Published Rise/Fall Time (Approx.) t_r/t_f	Principal Harmonic Content $f = 1/(\pi^{[a]} t_r)$	Typical Frequencies Observed as EMI (10^{th} *harmonic*) $f_{max} = 10^{[a]} f$
74L xxx	31–35 ns	10 MHz	100 MHz

74C xxx	25–60 ns	13 MHz	130 MHz
74HC xxx	13–15 ns	24 MHz	240 MHz
74 xxx	10–12 ns	32 MHz	320 MHz
(flip-flop)	15–22 ns	21 MHz	210 MHz
74LS xxx	9.5ns	34 MHz	340 MHz
(flip-flop)	13–15 ns	24 MHz	240 MHz
74H xxx	4–6 ns	80 MHz	800 MHz
74S xxx	3–4 ns	106 MHz	1.1 GHz
74HCT xxx	5–15 ns	64 MHz	640 MHz
74ALS xxx	2–10 ns	160 MHz	1.6 GHz
74ACT xxx	2–5 ns	160 MHz	1.6 GHz
74F xxx	1.5–1.6 ns	212 MHz	2.1 GHz
ECL 10K	1.5 ns	212 MHz	2.1 GHz
ECL 100K	0.75 ns	424 MHz	4.2 GHz
BTL	1.0 ns[a]	318 MHz	3.2 GHz
LVDS	0.3 ns[a]	1.1 GHz	11 GHz
GaAs	0.3 ns[a]	1.1 GHz	11 GHz
GTL+ (Pentium)	0.3 ns[a]	1.1 GHz	11 GHz
[a]These are minimum edge rate values.			

A fairly accurate rule-of-thumb in calculating *actual* edge transition values for minimum and maximum value is as follows:

- For maximum edge rate transition time, multiply the typical value by 1.2.
- For minimum edge rate transition time, multiply the typical value by 0.6.

This calculation will get one in the ballpark for design purposes related to actual edge rate values. The vendor of the device should be consulted for the real edge rate transition value, if not specified within the data sheet. The vendors *themselves* may not know the actual value.

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Chapter 3: Bypassing and Decoupling

OVERVIEW

Bypassing and decoupling refer to energy transfer from one circuit to another, in addition to enhancing the quality of the power distribution system. Three areas are of primary concern: power and ground planes, components, and internal power connections.

Decoupling is a means of overcoming physical and time constraints caused by digital circuitry switching logic levels. Digital logic usually involves two possible states, "0" or "1." Some conceptual devices may not be binary but ternary. The setting and detection of these two states are achieved with switches internal to components that determine whether the device is to be at logic LOW or logic HIGH. There is a finite time period for the device to make this determination. Within this window, a margin of protection is provided to guarantee against false triggering. Moving the logic switching state near the trigger level creates a degree of uncertainty. If we add high-frequency noise, the degree of uncertainty increases and false triggering may occur.

Decoupling is also required to provide sufficient dynamic voltage and current levels for proper operation of components during clock or data transitions when all component signal pins switch simultaneously under maximum capacitive load. Decoupling is accomplished by ensuring that a low-impedance power source is present. Because decoupling capacitors have increasingly low impedance at high frequencies, up to the point of self-resonance, high-frequency noise is effectively diverted from the power distribution network, whereas low-frequency RF energy remains relatively unaffected. Optimal implementation is achieved using capacitors for a specific application: bulk, bypass, and decoupling. All capacitor values must be calculated for a specific function. In addition, the dielectric material of the capacitor must be properly selected and not be left to random choice from past usage, experience, or rules-of-thumb.

Three common uses of capacitors follow. Of course, a capacitor may also be used in other applications such as timing, wave shaping, integration, and filtering.

Decoupling. Removes RF energy injected into the power distribution network from high-frequency components consuming power at the speed at which the device is switching. Decoupling capacitors also provide a localized source of DC power for devices and components, and is particularly useful in reducing peak current surges propagated across the board.

Bypassing. Diverts unwanted common-mode RF noise from components or cables coupling from one area to another. This is essential in creating an AC shunt to remove undesired energy from entering susceptible areas, in addition to providing other functions of filtering (bandwidth limited).

Bulk. Helps maintain constant DC voltage and current levels to components when all signal pins switch simultaneously under maximum capacitive load. It also prevents power dropout due to *dI*/*dt* surges generated by components.

An ideal capacitor has no losses in its conductive plates and dielectric. Current is always present between two parallel plates. Because of this current, an element of inductance is associated with the parallel plate configuration. Because one plate is charging while its counterpart is discharging, a mutual coupling factor is added to the overall performance and operation of the capacitor.

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3.1 REVIEW OF RESONANCE

All capacitors consist of an *RLC* circuit, where *L* = inductance related to lead length and body construction, *R* = resistance in the leads, and *C* = capacitance. A schematic representation of a capacitor is shown in Fig. 3.1. At a calculable frequency, the series combination of *L* and *C* becomes resonant, providing very low impedance and effective RF energy shunting at resonance. At frequencies above self-resonance, the impedance of the capacitor becomes increasingly inductive, and bypassing or decoupling becomes less effective. Hence, bypassing and decoupling are affected by the lead inductance of the capacitor (surface mount, radial, or axial styles), the trace length between the capacitor and component, feed-through pads (or vias), and so forth.

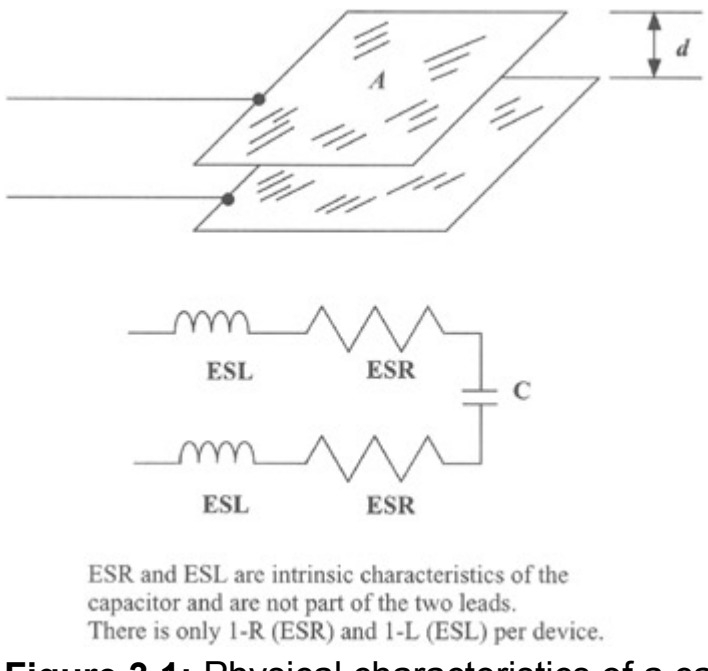

Figure 3.1: Physical characteristics of a capacitor with leads.

Before discussing bypassing and decoupling, a review of resonance is provided. Resonance occurs in a circuit when the reactive value difference between the inductive and capacitive vector is zero. This is equivalent to saying that the circuit is purely resistive in its response to AC voltage. Three types of resonant circuits are common, although more types of circuits exist.

- Series resonance
- Parallel resonance
- Parallel *C*-series *RL* resonance

Resonant circuits are frequency selective because they pass RF current at certain frequencies than at other frequencies. A series *LCR* circuit will pass a selected frequency (measured across *C*) if *R* is high and source resistance is low. If *R* is low and the source resistance is high, the circuit will reject the chosen frequency. A parallel resonant circuit placed in series with a load will reject a specific frequency.

3.1.1 Series Resonance

The overall impedance of a series *RLC* circuit is defined by

$Z = \sqrt{R^2 + (X_L - X_C)^2}$. If an *RLC* circuit is to behave resistively, the value can be calculated (Fig. 3.2) where ω (2π*f*) is identified as the *resonant angular frequency*.

$$X_L = X_C$$

$$\omega L = \frac{1}{\omega C}$$

$$\omega = \frac{1}{\sqrt{LC}}$$

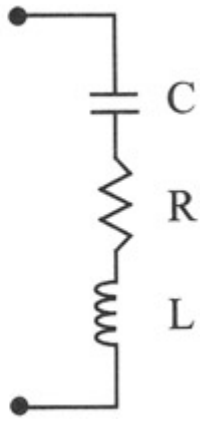

Figure 3.2: Series resonant circuit.

With a series *RLC* circuit at resonance,

- Impedance is at a minimum.
- Impedance equals resistance.
- The phase angle difference is zero.
- Current is at a maximum.
- Power transfer (*IV*) is at a maximum.

3.1.2 Parallel Resonance

A parallel *RLC* circuit behaves as shown in Fig. 3.3. The resonant frequency is the same as for a series *RLC* circuit.

$$\omega L = \frac{1}{\omega C}$$

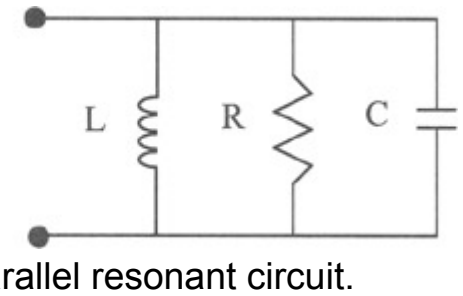

Figure 3.3: Parallel resonant circuit.

With a parallel *RLC* circuit at resonance,

- Impedance is at a maximum.
- Impedance equals resistance.
- The phase angle difference is zero.
- Current is at a minimum.
- Power transfer (*IV*) is at a minimum.

This circuit configuration produces a resonance when inductance, *L*, equals capacitance, *C*. The impedance would go to infinity if the resistance equaled zero. The resistor can be of significant benefit under certain conditions to prevent parallel resonance.

If the resistance value is too high, the equivalent series resistance of the component will exceed the inductance values at the resonant frequency point. If the resistance is just right, inductive impedance is equal to the resistance, again at the resonant frequency. Resonance is the condition under which the inductive impedance is equal to the capacitive impedance.

3.1.3 Parallel C-Series RL Resonance (Antiresonant Circuit)

Practical resonant circuits generally consist of an inductor and a capacitor in parallel. The inductor will possess some resistance. The equivalent circuit is shown in Fig. 3.4. The resistance in the inductive branch may be a

discrete element or the internal resistance of the physical inductor.

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{L}\right)^2} \approx \frac{1}{\sqrt{LC}} \quad [R \ll \omega_r L]$$

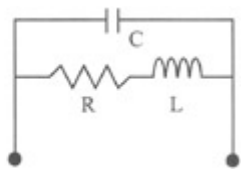

Figure 3.4: Parallel C—series RL resonant circuit.

At resonance, the capacitor and inductor trade the same stored energy on alternate half cycles. When the capacitor discharges, the inductor charges, and vice versa. At the antiresonant frequency, the tank circuit presents high impedance to the primary circuit current, even though the current within the tank is high. Power is dissipated only in the resistive portion of the network.

The antiresonant circuit is equivalent to a parallel *RLC* circuit whose resistance is Q^2R.

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Chapter 3 - Bypassing and Decoupling

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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3.2 PHYSICAL CHARACTERISTICS

3.2.1 Impedance

The equivalent circuit of a capacitor was shown in Fig. 3.1. The actual impedance value of this capacitor is

(3.1) $$|Z| = \sqrt{R_s{}^2 + \left(2\pi fL - \frac{1}{2\pi fC}\right)^2}$$

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where Z = impedance (Ω)

R_s = equivalent series resistance—ESR (Ω)

f = frequency (Hz)

L = equivalent series inductance—ESL (H)

C = capacitance (F)

From this equation, $|Z|$ exhibits a minimum impedance value at a specific resonant frequency, f_o, such that

(3.2) $$f_o = \frac{1}{2\pi\sqrt{LC}}$$

Get MathML

In reality, the impedance equation (Eq. 3.1) reflects hidden parasitics that are present when we take into account ESL and ESR.

Equivalent series resistance (ESR) is a term referring to resistive losses in a capacitor. This loss consists of the distributed plate resistance of the metal electrodes, the contact resistance between internal electrodes, and the external termination points. Note that skin effect at high frequencies increases this resistive value in the leads of the component. Thus, high-frequency "ESR" is higher in equivalence than a DC equivalent level.

Equivalent series inductance (ESL) is the loss element; however, by definition, any (ideal) reactive element is lossless. It stores and returns energy but does not dissipate it. Energy dissipation (losses) only occurs in resistive elements. The value of ESL in a capacitor must keep to a minimum the restriction of current flow within a device package. The tighter the restriction, the higher the current density and the higher the ESL. The ratio of width to length must be taken into consideration to minimize this parasitic element.

Examining Eq. (3.1), we have a variation of the same equation with ESR and ESL substituted in, shown in Eq. (3.3).

(3.3) $$|Z| = \sqrt{(ESR)^2 + (X_{ESL} - X_C)^2}$$

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where $X_{ESL} = 2\pi f(ESL)$

$$X_C = \frac{1}{2\pi f C}$$

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For certain types of capacitors, with regard to dielectric material, the capacitance value varies with temperature and DC bias. Equivalent series resistance varies with temperature, DC bias, and frequency, whereas ESL remains fairly unchanged.

In order for an ideal capacitor to exist, the device needs to have a high capacitance, *C*, and a low inductance, *L*, such that the overall impedance will not increase at higher frequencies. For this reason, power and ground plane structures are optimal in providing low-impedance decoupling within a PCB over discrete components.

3.2.2 Capacitor Types

There are various types of capacitor families, all with different features and performance capabilities. A brief summary of commonly used capacitors is detailed in Table 3.1.

Table 3.1: Summary of Various Capacitor Types

Open table as spreadsheet

Electrolytic	Large capacitance value Large physical size Low ESL and ESR Low end of life capacitance value
Tantalum	Capacitance value from 1 µF to 1000 µF Medium to small package size Large range of ESL, some with low ESR
Ceramic	Very small capacitance values Small package size Very low ESR Lowest cost with the highest reliability
Capacitor arrays	Ceramic capacitors dielectric Multiple contacts per device package Very low ESL High cost

3.2.3 Energy Storage

Decoupling capacitors ideally should be able to supply all the current necessary during a state transition of a logic device to ensure functionality, described by Eq. (3.4). Use of decoupling capacitors on two-layer boards also reduces power supply ripple.

(3.4)
$$C = \frac{\Delta I}{\Delta V / \Delta t}$$

Get MathML

For example, $\frac{20\text{ mA}}{100\text{ mV}/5\text{ ns}} = 0.001\ \mu\text{F}$ or 1000 pF

where ΔI = current transient

ΔV = allowable power supply voltage change (ripple)

Δt = switching time

Note that for ΔV, EMI requirements are usually more demanding than component supply needs. The ΔI requirement is usually unknown or not provided by the device manufacturer. The value of Δt is usually given as "typical" or "maximum," but rarely as "minimum," which is the primary variable of interest.

The response of a decoupling capacitor is based on a sudden change in demand for current. It is useful to interpret the frequency domain impedance response in terms of the capacitor's ability to supply current. This charge transfer ability is also for the time domain function for which the capacitor is generally selected. The low-frequency impedance between the power and ground planes indicates how much voltage on the board will change when experiencing a relatively slow transient. This response is an indication of the time-average voltage swing experienced during a fast transient. With low impedance, more current is available to the components under a sudden change in voltage. High-frequency impedance indicates how much current the board can initially supply in response to a fast transient. Boards with the lowest impedance above 100 MHz can supply the greatest amount of current (for a given voltage change) during the first few nanoseconds only from a sudden transient surge.

Current requirements for each component must be identified to properly assess decoupling and power distribution requirements. Current requirements are categorized as follows:

- *Quiescent:* The steady-state current level required for normal operation.
- *Output capacitive load:* Capacitive load charging current that the driver must send to a load.
- *Transmission line load:* Transmission line load current required to propagate an electromagnetic field from source to load. This requires a slower, lower amplitude time period to keep the line charged until all of the reflections are over.
- *Device output charge:* The amount of output change switching current available.
- *Cyclic switching:* Component decoupling capacitance recharge current.

The underlying component of the power distribution system is DC distribution. By definition, this component is time invariant. When analyzing the AC power requirements, the DC voltage drop, or noise margin budget is usually considered *only* to determine the voltage drop budget allowance for the AC component.

3.2.4 Resonance

When selecting bypass and decoupling capacitors, storage capacity and discharge frequency must be calculated based on the logic family and clock speed of the circuit (self-resonant frequency). One must select a capacitance value based on the impedance that the capacitor presents to the circuit. A capacitor remains capacitive up to its self-resonant frequency. Above self-resonance, the capacitor starts to appear as an inductor due to lead length and trace inductance. Inductance minimizes the ability of the capacitor to decouple or remove RF energy that exists between power and ground. Table 3.2 illustrates the self-resonant frequency for two types of ceramic capacitors, one with standard 0.25 in. leads (radial or axial) and the other surface mount. The self-resonant frequency of surface mount (SMT) capacitors is always higher, although interconnect inductance may obviate this benefit. Interconnect inductance includes routed traces and the bond wires internal to a component package. Depending on the type of product being designed, as well as on the frequency of operation, a change of inductance in the picohenry range may be too much to tolerate.

Table 3.2: Approximate Self-Resonant Frequency of Various Capacitors (lead-length dependent)

Open table as spreadsheet

Capacitor Value	Through-Hole[a] 0.25-in. Leads	Surface Mount[b] (0805)
1.0 µf	2.6 MHz	5 MHz
0.1 µf	8.2 MHz	16 MHz
0.01 µf	26 MHz	50 MHz
1000 pF	82 MHz	159 MHz
500 pF	116 MHz	225 MHz
100 pF	260 MHz	503 MHz
10 pF	821 MHz	1.6 GHz

[a]For through-hole, L = 3.75 nH (15 nH/in.).

[b]For surface mount, L = 1 nH.

When selecting a capacitor, one should consider not only the self-resonant frequency but the dielectric material as well. The most commonly used material is Z5U (barium titanate ceramic). This material has a high dielectric constant that allows small capacitors to have large capacitance values with self-resonant frequencies from 1 MHz to 20 MHz, depending on design and construction. Above self-resonance, performance of Z5U decreases as the loss factor of the dielectric becomes dominant, which limits its usefulness to approximately 50 MHz.

Another dielectric material commonly used is NPO (strontium titanate). This material has a much better high-frequency performance owing to its low dielectric constant. Capacitors using this material are unsuitable for decoupling below 10 MHz. NPO is also a more temperature-stable dielectric. Capacitance value (and self-resonant frequency) is less likely to change when the capacitor is subjected to changes in ambient temperature.

A problem observed when Z5U and NPO are provided in parallel is that the higher dielectric material, Z5U, can damp the resonance of the more frequency-stable, low-dielectric constant material, NPO. For EMI problems below 50 MHz, it is better to use only a good, low-inductance Z5U (or equivalent) capacitor. This is because Z5U combines excellent low-frequency decoupling with reduction in radiated emissions.

An example of the magnitude of impedance presented to the PCB, based on dielectric material usage, is presented in Fig. 3.5.

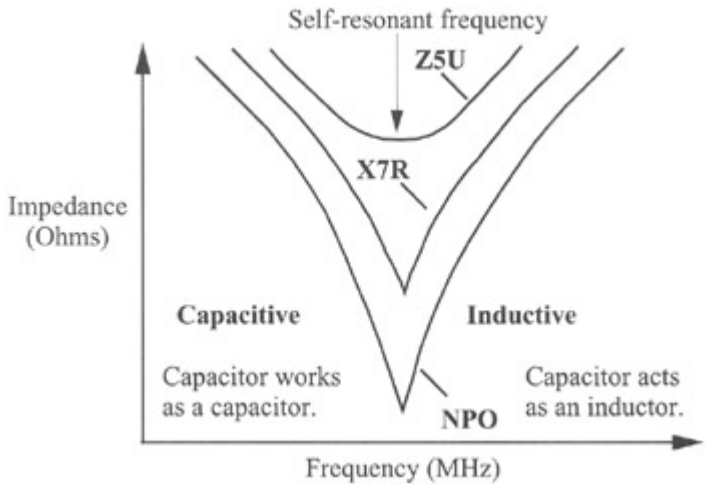

Figure 3.5: Magnitude of impedance due to different dielectric material.

Through-hole capacitors are nothing more than surface mount devices with leads attached. A typical leaded capacitor has on the average approximately 2.5 nH of inductance for every 0.10 in. of lead length. Surface mount capacitors average 1 nH *total* lead-length inductance. This inductance is based on typical trace dimensions and will vary with width, thickness, and length.

An inductor does not change its resonant response like a capacitor; instead, the *magnitude* of the device's impedance will change as frequency changes. Parasitic capacitance between the windings of the inductor, however, can cause a parallel resonance to occur, which may alter the desired response. The higher the frequency of the circuit, the greater the magnitude of the impedance changes. RF current traveling through this impedance causes a RF voltage potential difference between input and output. Consequently, RF current is developed within the device, described by Ohm's law, $V_{rf} = I_{rf} * Z$ (see Chapter 2). An important design concern when selecting and implementing capacitors for decoupling deals with lead inductance. SMT capacitors perform better at higher frequencies than radial or axial capacitors because of lower internal lead inductance. Table 3.3 shows the magnitude of impedance of a 15 nH inductor versus frequency ($Z = 2\pi fL$).

Table 3.3: Magnitude of Impedance of a 5-nH Inductor versus Frequency

➪ Open table as spreadsheet

Frequency (MHz)	Z (ohms)
0.1	0.01
0.5	0.05
1.0	0.10
10.0	1.0
20.0	1.9
30.0	2.8
40.0	3.8
50.0	4.7
60.0	5.7
70.0	6.6
80.0	7.5
90.0	8.5
100.0	9.4

Figure 3.6 shows the self-resonant frequency of through-hole capacitors with 0.25 in. (6.4 mm) leads, either radial or axial. Capacitors are capacitive until they approach self-resonance (null point, or low value of impedance) before going inductive. Above the point where capacitors go inductive, they proportionally cease to function for RF decoupling; however, they may still be the best source of charge for the device, even at frequencies where they are inductive. This is because the internal bond wire from the capacitor's plates to its mounting pad (or pin) must be taken into consideration. Inductance is what causes capacitors to become less useful at frequencies above self-resonance for decoupling purposes.

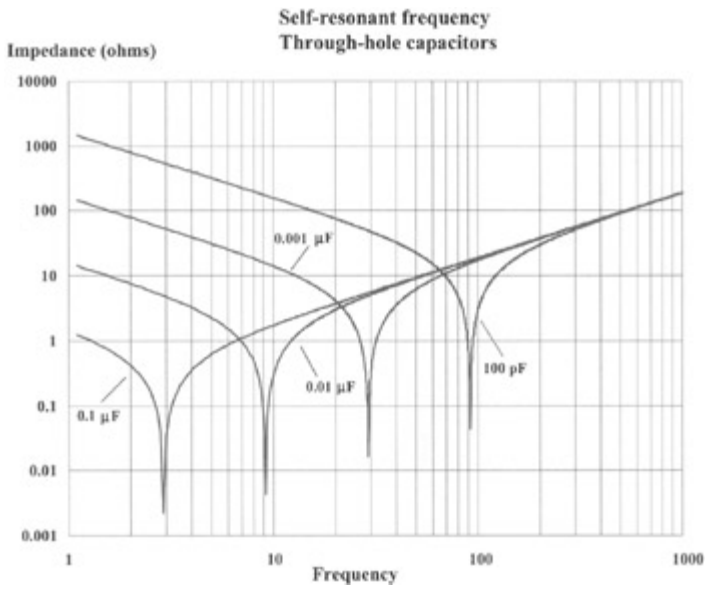

Figure 3.6: Self-resonant frequency of through-hole capacitors.

Certain logic families generate a large amount of RF energy throughout the frequency spectrum. The energy developed by components is generally higher in frequency than the self-resonant range a decoupling capacitor presents to the circuit. For example, a 0.1 µF capacitor will usually not provide adequate decoupling for RF currents associated with ACT or F logic devices, although performance for slower speed logic is assured. A 0.001 µF capacitor is a more appropriate choice due to a higher self-resonant frequency of operation that most closely matches the component with its faster edge rate (0.8–2.0 ns minimum) and frequency of operation, typical of higher-speed devices.

Compare the difference between through-hole and surface mount (SMT). SMT components have less lead inductance. The self-resonant frequency of operation is higher than the through-hole device. Figure 3.7 illustrates a plot of the self-resonant frequency of various values of ceramic capacitors. All capacitors in the figure have the same lead inductance value for comparison purposes.

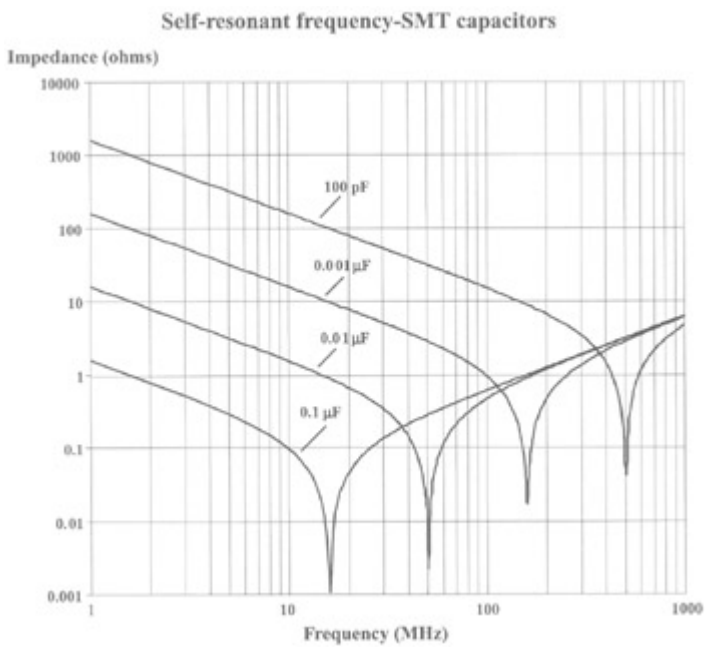

Figure 3.7: Self-resonant frequency of SMT capacitors.

Effective decoupling mandates that a minimal amount of inductance be associated with a capacitor. Even a small amount of inductance may change the self-resonant frequency of operation significantly, making the capacitor ineffective for optimal or desired performance. Although an engineer may take into consideration trace and lead inductance during the design cycle, a PCB designer sometimes locates passive components where space is available. In some cases, auto-placement of vias from the power and ground planes to the capacitor pads occurs with a trace between pad and via. Inductance will always be present internal to the capacitor's package, trace length between capacitor and component, via interconnect, lead-bond wires internal to the component, or other interconnect structures provided within the PCB assembly.

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Chapter 3 - Bypassing and Decoupling

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by Mark I. Montrose

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3.3 CAPACITORS IN PARALLEL

It is common practice during a product design to make provisions for parallel decoupling of capacitors with the intent of providing a greater spectral distribution of performance while minimizing switching noise induced within the power and ground distribution network. Board-level-induced noise, sometimes identified as "delta-I," is a primary cause of RF emissions. This delta-I noise is mistakenly referred to as ground bounce. In reality, ground bounce is a difference of voltage potential internal to a component's package between the die and external mounting pads. This internal voltage potential difference occurs across the lead-bond wires. When parallel decoupling is provided, one must not forget that a third capacitor exists—the power and ground planes.

When DC power is consumed by digital components switching logic states, a momentary surge occurs within the power distribution network. Decoupling provides a localized point source charge to prevent this surge from disrupting the power supply network. By keeping the voltage and ground level at a stable reference point, false logic switching events are prevented.

Research on the effectiveness of multiple decoupling capacitors shows that parallel decoupling may not be significantly effective and that at high frequencies, only a 6 dB improvement may occur over the use of a single larger-value capacitor. Although 6 dB appears to be a small number for suppression of RF current, it may be all that is required to bring a noncompliant product into compliance with international EMI specifications.

> Above the self-resonant frequency of the larger value capacitor where its impedance increases with frequency (inductive), the impedance of the smaller capacitor is decreasing (capacitive). At some point, the impedance of the smaller value capacitor will be smaller than that of the larger capacitor, and will dominate, thereby giving a smaller net impedance than that of the larger value capacitor alone [2].

This 6 dB improvement occurs as a result of lower lead and device-body inductance provided by two capacitors in parallel. Two parallel sets of leads provide a greater trace width than would be available if only one capacitor was used. With a wider trace width, there is less lead inductance. This reduced lead inductance is a significant reason why parallel decoupling works, as well as it does. However, one disadvantage does exist with parallel decoupling.

Figure 3.8 shows a plot of two bypass capacitors, 0.01 µF and 100 pF, both individually and in parallel. The 0.01 µF capacitor is self-resonant at 14.85 MHz. The 100 pF capacitor has its self-resonant frequency at 148.5 MHz. At 110 MHz, there is a large increase in the magnitude of impedance owing to this parallel combination. The 0.01 µF capacitor has already gone inductive, while the 100 pF capacitor is still capacitive. We now have both *L* and *C* in resonance at 110 MHz, causing an antiresonant effect. An antiresonant frequency is exactly what we do *not* want in a PCB, if compliance to EMI requirements is required. At this particular frequency, any harmonic of a clock transition will be observed as a powerful, transmitting signal. For this example, the third harmonics of a 36 MHz oscillator is 108 MHz.

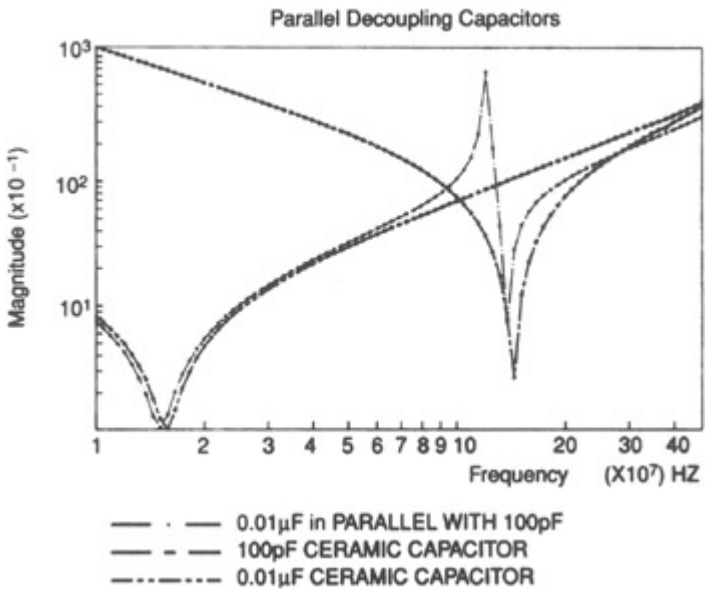

Figure 3.8: Resonant effect from two capacitors in parallel. (Source: Ref [2]. Reprinted by permission—IEEE Press.)

> Between the self-resonant frequency of the larger value capacitor, 0.01 µF, and the self-resonant frequency of the smaller value capacitor, 100 pF, the impedance of the 0.1 µF capacitor is essentially inductive, whereas the impedance of the 100 pF capacitor is capacitive. In this frequency range there exists a parallel resonant *LC* circuit. We should therefore expect to find an infinite impedance from the parallel combination. Around this resonant point, the impedance of the parallel combination is actually larger than the impedance of either isolated capacitor [2].

Figure 3.8 shows that at 500 MHz, the impedances of the individual capacitors are virtually identical. The parallel impedance is only 6 dB lower. This 6 dB improvement is only valid over a limited frequency range from about 120 to 160 MHz.

To remove RF current generated by digital components switching all signal pins simultaneously, and if use of parallel decoupling is desired, a common practice is to place two capacitors in parallel (e.g., 0.1 µF and 0.001 µF) immediately adjacent to each power pin. If parallel decoupling is used within a layout, one must be aware that the capacitance values should differ by two orders of magnitude, or 100x. This magnitude difference is required because the two capacitors will form a resonant tank circuit (capacitor plates and interconnect inductance).

To optimize the effects of parallel bypassing and to allow use of only one capacitor, reduction in lead inductance is required. A finite amount of inductance will always exist when installing the capacitor on the board. Note that lead inductance must also include the inductance value and physical length of the via that connects the capacitor to the planes. The shorter the lead length, the greater the performance. In addition, some manufacturers provide capacitors with significantly reduced ESL internal to the capacitor package.

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3.4 POWER AND GROUND PLANES

A benefit of using multilayer assemblies is the ability to have a power and ground plane distribution network to enhance the overall performance of system operation. This performance exists by virtue of having a low-impedance path between the power source and component. A low-impedance path allows for a minimal amount of voltage drop to be present for the overall assembly, power supply to components, and component to component. If an imbalance exists within the power distribution network, common-mode RF energy will be developed.

The physical relationship of these two planes creates one large capacitor—two parallel plates separated by a dielectric. This capacitor generally provides adequate decoupling for most low-speed (slower edge rate) designs; however, additional signal or plane layers add cost to the overall assembly. If components have signal edge transitions (t_r or t_f) slower than 10 ns (e.g., standard TTL logic), use of high-performance, high self-resonant frequency discrete decoupling capacitors may not be required. Bulk capacitors are still needed, however, to maintain proper voltage levels to ensure proper operation of the design.

Depending on the thickness of the core material, the dielectric constant value, and the placement of the planes within a board stackup, various values of capacitance can exist. Network analysis, mathematical calculations or modeling will reveal the actual capacitance of the power and ground plane structure. Proper analysis determines total impedance of the complete PCB, including the effects of the power and ground planes, together with all discrete decoupling capacitors.

Table 3.4 shows some frequency response characteristics of various capacitors.

Table 3.4: Typical Usage of Capacitor Families and Operating Range

Open table as spreadsheet

Power supply DC/DC converters	DC to 2 kHz
Large capacitors Electrolytic or tantalum	2 kHz to 1 MHz
Small capacitors Tantalum or ceramic	1 MHz to 50 MHz
PCB planes Between the power and ground planes	50 MHz and up
Integrated circuit package Between power and ground planes	Above 100 MHz
Inside the integrated circuit (the silicon die) Thin oxide capacitor	Above 500 MHz

3.4.1 Calculating Power and Ground Plane Capacitance

This value of planar capacitance is estimated by Eqs. (3.5) and (3.6). Actual capacitance is generally less than the calculated value owing to parasitics that cannot be anticipated or included within these equations.

(3.5)
$$C = \frac{\varepsilon_o \varepsilon_r A}{d} = \frac{\varepsilon A}{d}$$

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where C = capacitance between the power and ground planes (pF)

ϵ_o = permittivity of free space, 1/36 π*10^{-9} F/m = 8.85*10^{-12} F/m = 8.85 pF/m

ϵ_r = relative permittivity of the medium between the plates, typically, $\approx$ 4.5 (varies for linear material, usually between 1 and 10)

A = area of the parallel plates (m^2)

d = separation of the plates (m)

Introducing relative permittivity, ϵ_r, of the dielectric material, and the value of ϵ_o, the permittivity of free space, one can obtain the capacitance of the parallel-plate capacitor, namely, the power and ground plane.

Equation (3.5) is simplified to Eq. (3.6).

(3.6)
$$C_{pp} = k\frac{\varepsilon_r A}{d}$$

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where C_{pp} = capacitance of parallel plates (pF)

k = conversion constant incorporating ϵ_o (0.2249 for in., 0.884 for cm)

ϵ_r = dielectric constant of the board material (vacuum = 1, FR-4 material = 4.1 to 4.7)

A = total area between the parallel plates (square in. or square cm)

d = distance spacing between the plates (in. or cm)

One caveat in solving this equation is that the inductance caused by antipads (holes for through-vias) in the power and ground planes can minimize the theoretical effectiveness of using power and ground plane capacitance for decoupling.

Because the power planes are efficient as a decoupling capacitor, use of discrete components may not be required for standard TTL or slow-speed logic. This optimum efficiency exists, however, only when the power and ground planes are closely spaced—less than 0.010 in. (0.25 mm), with 0.005 in. (0.13 mm) preferred for high-speed applications [3].

Other factors to consider when using power and ground planes as a decoupling capacitor is the self-resonant frequency of the overall assembly. If the self-resonant frequency of the power and ground planes is the same as the self-resonant frequency of the lumped total of all discrete capacitors provided, there will be a sharp resonance where these two frequencies meet. No longer will there be a wide spectral distribution of decoupling. If a clock harmonic is at the same frequency as this sharp resonance, the board will act as if very little decoupling is present. When this situation develops, the PCB may become an unintentional radiator, along with possible noncompliance with EMI requirements. Should this

occur, additional decoupling capacitors (with a different self-resonant frequency) will be required to shift the resonance of the PCB's power and ground planes.

One simple method to change the self-resonant frequency of the power and ground planes is to change distance spacing between the planes or their physical size (area). Increasing or decreasing the height separation and relocation within the layer stackup, or making the planes a different physical size will change capacitance value. Equations (3.5) and (3.6) illustrate this principle. One disadvantage of using this design technique is that the impedance of the signal routing layers may also change, which is a performance concern. A designer must make compromises during layout, especially if a high level of decoupling is more important than impedance control for signal traces. Multilayer PCBs generally have a self-resonant frequency between 200 and 400 MHz.

In the past, slower speed logic devices fell well below the spectrum of the self-resonant frequency of the PCB's power and ground plane structure. The logic devices used in newer, high-technology designs easily approach or exceed this critical resonant frequency. When both the impedance of the power/ground planes and individual decoupling capacitors approach the same resonant frequency, severe performance deterioration can occur. This degraded high-frequency impedance will result in EMI. Thus, the assembled PCB becomes an unintentional transmitter. The PCB is not really the transmitter; rather, the highly repetitive circuits or clocks are the cause of RF energy present that radiates or couples to unintentional circuits. Because decoupling will not solve this type of problem (owing to the resonance of the decoupling effect), system-level containment measures will be required.

3.4.2 Combined Effects of Planar and Discrete Capacitors

The effects of internal power and ground planes inside the PCB are not considered in Fig. 3.8. However, multiple bypassing effects are illustrated in Fig. 3.9. Power and ground planes have very little inductance and practically no ESR (equivalent series resistance). Use of power planes as a decoupling capacitor helps reduce RF energy generally in the higher frequency ranges.

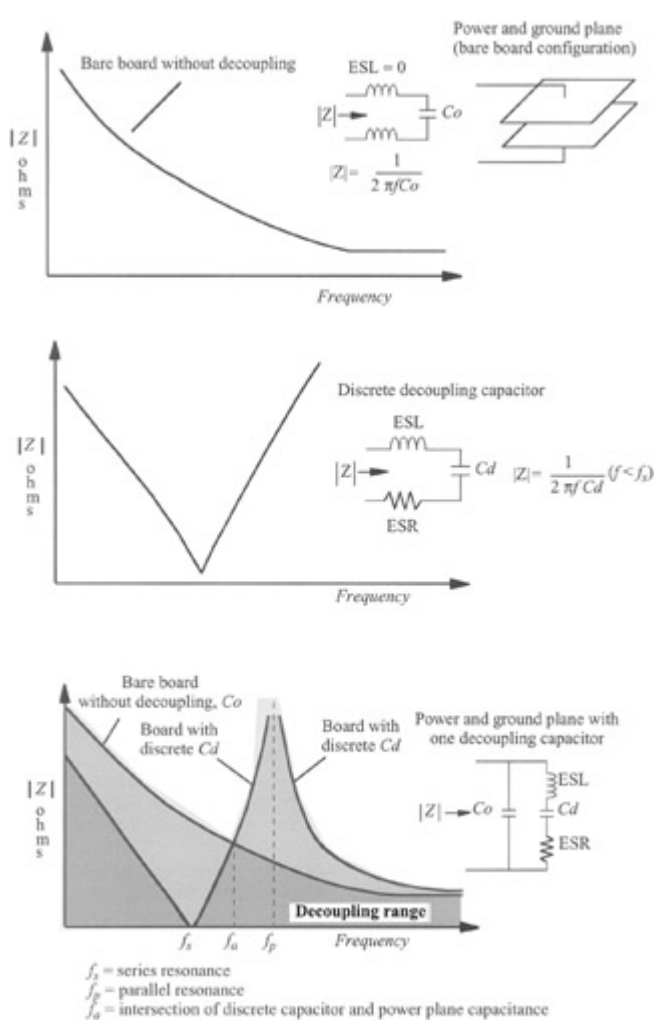

Figure 3.9: Decoupling effects of power ground planes with discrete capacitors.

On most multilayer boards, the inductance of the planes between two physical locations is significantly less than 1 nH. Conversely, lead and/or trace inductance (the inductance associated with a trace connecting a

component to its respective termination point plus the via) is typically 2.5 to 10 nH [4]. Primarily for this reason, routing traces between the capacitor and component is not desired!

Although good distributive capacitance exists when using a power and ground plane, adjacent close stacking of these planes plays a critical part in the overall assembly. If two sets of power and ground planes are present, for example, +5V/ground and +3.3V/ground, both with different dielectric spacing between the two planes, multiple decoupling capacitors can be built internal to the board. With proper selection of layer stackup, both high-frequency and low-frequency decoupling can be achieved without use of any discrete devices! To expand on this concept, a technology known as buried capacitance is finding use in high-technology products that require high-frequency decoupling.

3.4.3 Buried Capacitance

Buried capacitance[1] is a patented manufacturing process in which the power and ground planes are separated by a 0.001 in. (0.025 mm) dielectric. With this small dielectric spacing, decoupling is effective up to 200–300 MHz. Above this frequency range, use of discrete capacitors is required to decouple components that operate above the cutoff frequency of the buried capacitance. The important item to remember is that the closer the distance spacing is between the power and ground planes, the better the decoupling performance. Although buried capacitance may eliminate the employment and cost of discrete components, use of this technology may far exceed the cost of all discrete components that are to be removed. Figure 3.10 illustrates the concept of buried capacitance.

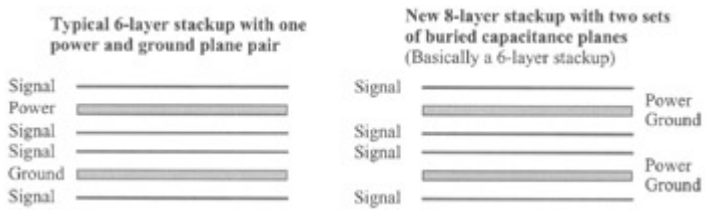

Figure 3.10: Implementation of buried capacitance.

To better understand the concept of buried capacitance, the power and ground planes should be considered as pure capacitance at low frequencies with very little inductance. These planes are an equal-potential surface with no voltage gradient except for a small DC voltage drop. This capacitance is calculated simply as the area divided by thickness times permittivity, Eq. (3.5). For a 10 in. square board, with 1-mil spacing between layer, FR-4 dielectric (ϵ_r = 4.5), we have a capacitor with a value of 45 nF (0.045 μF). Typical value of capacitance for buried capacitance is 506 pF/in^2. The capacitance of two planes is less than buried capacitance. Vias will cause a reduction in total capacitance. Because copper is removed from each plane, a small amount of capacitance is also removed from the final assembly. The magnitude of this concern is minimal for most product designs and can be ignored for all but extremely complicated systems.

Decoupling capacitance (buried capacitance) is increased because the distance spacing between the planes *(d)* in the denominator is decreased. The power and ground planes are the means of distributing power. Reducing dielectric thickness is highly effective for high-frequency decoupling.

Buried capacitance is a special manufacturing process, where material is imaged onto a substrate using the power and ground plane artwork. The lamination is an integral part of the assembly. By sharing capacitance between layers, sufficient instantaneous distributed capacitance with minimal inductance will be present. It is to be noted that buried capacitance has a dielectric breakdown value that is less than a standard power and ground plane assembly. Use in high-voltage applications may not be desired.

The use of discrete decoupling capacitors may not be necessary when buried capacitance is used. With fewer discrete devices, less inrush surge current is required, which is beneficial to minimizing board-induced noise

voltage, ground bounce, and development of common-mode energy. Boards may radiate RF energy because of *excessive* usage of discrete decoupling capacitors located throughout the PCB!

[1]Buried capacitance is a registered trademark of HADCO Corporation (which purchased Zycon Corporation, developers of this technology).

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Chapter 3 - Bypassing and Decoupling

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

IEEE Press © 2000

Recommend this title? yes no

3.5 PLACEMENT

3.5.1 Power Planes

Multilayer PCBs contain one or more pair of voltage and ground planes. These planes function as a low-inductance capacitor, preventing creation of RF currents generated from components switching logic states. Multiple chassis ground connections to all ground planes minimize voltage gradients between board, chassis, and board layers. These gradients also are a major source of common-mode RF fields. This is in addition to sourcing RF currents to chassis ground. In many cases, multiple ground connections to chassis are not always possible, especially in card cage designs. In such situations, care must be taken to analyze and determine where RF loop currents occur.

Power planes that are located next to ground planes provide for enhanced flux cancellation in addition to decoupling RF currents created from power fluctuations owing to components injecting noise into the network. Components switching logic states cause a current surge during the transition. This current surge places a strain on the power distribution network. An image plane is a solid copper plane at voltage or ground potential located adjacent to a signal routing plane. RF currents present will mirror image themselves in this adjacent solid reference plane. This solid reference plane must not be isolated from the power distribution network [5]. To remove common-mode RF currents created within a PCB, all routing (signal) layers must be physically adjacent to an image plane. (For a detailed discussion of image planes, see Chapter 2.)

3.5.2 Equivalent Circuit Model of a PCB

Before determining where to locate decoupling capacitors, the physical structure of a PCB must be understood. Figure 3.11 shows the electrical equivalent circuit of a PCB assembly. In this figure, there are loops between power and ground caused by traces, IC wire bonds, lead frames of components, socket pins, component interconnect leads, and the lead length of the decoupling capacitor. The key to effective decoupling is to minimize R_2, L_2, R'_2, L'_2, R_3, L_3, R'_3, L'_3, R_4, L_4, R'_4, and L'_4. Placement of power and ground pins in the center of the component helps reduce R_4, L_4, R'_4, and L'_4. The impedance of the PCB must be minimized. The easiest way to minimize the resistive and inductive components of the PCB is to provide solid planes, which removes many of the inductive elements of the structure. To minimize inductance from component leads, use of SMT, ball grid arrays, and flip chips is preferred. With fewer lead-bond lengths from the die to PCB pad, overall impedance of the decoupling loop is also reduced.

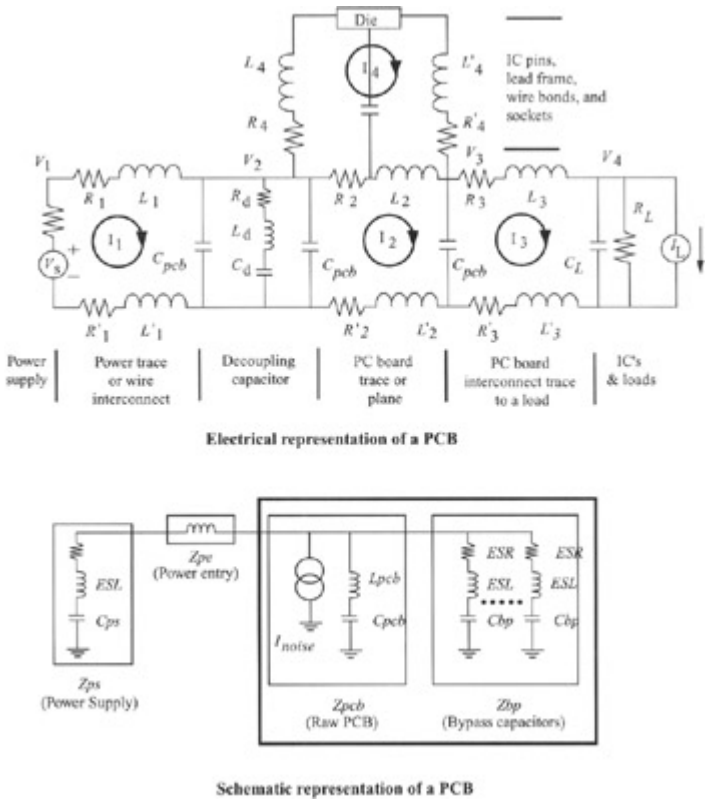

Figure 3.11: Equivalent representation of a PCB.

Figure 3.11 [1] makes it clear that EMI is a function of loop geometry and frequency. Hence, the smallest closed-loop area is desired. We acquire this small area by placing a local decoupling capacitor, C_d, for current storage adjacent to the power pins of the component. It is mandatory that the decoupling loop impedance be much lower than the rest of the power distribution system. This low impedance will cause high-frequency RF energy developed by both traces and components to remain almost entirely within this small loop area. Consequently, lower EMI emissions are developed.

If the impedance of the decoupling loop is smaller than the rest of the system, some fraction of the high-frequency RF energy will transfer, or couple, to the larger loop formed by the power distribution system. With this situation, RF currents are injected in the larger loop structure, and hence, higher EMI emissions are the result. This situation is illustrated in Fig. 3.12 [8].

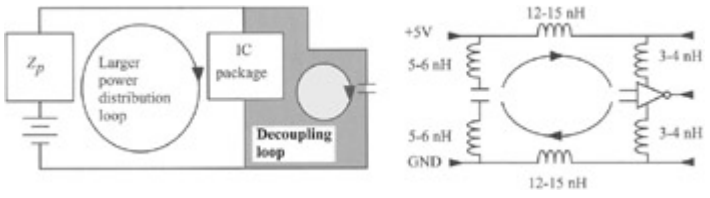

Figure 3.12: Power distribution model for loop control.

To summarize,

> The important parameter when using decoupling capacitors is to minimize lead inductance and to locate the capacitors as close as possible to the component.

3.5.3 Decoupling Capacitors

Decoupling capacitors must be provided for devices with edges transition rates faster than 2 ns and should be provided, placement wise, for every component. Making provisions for decoupling capacitor usage during layout is a necessity because future EMI analysis may indicate a requirement for these devices. During testing, it may be possible to determine that extra capacitors may be required. Having to add capacitors to an assembled board is difficult, if not impossible. Today, CMOS, ECL, and other fast logic families require additional discrete decoupling, besides the power and ground planes.

If a decoupling capacitor must be provided to a through-hole component after assembly, retrofit can be performed. Several manufacturers provide a decoupling capacitor assembly using a flat, level construction that resides between the component and PCB. This flat pack shares the power and ground pins of the components. Because these capacitors are flat in construction, lead-inductance is much less compared to capacitors with

discrete radial or axial leads. Since the capacitor and component share the same power and ground pins, R_2, L_2, R'_2, and L'_2 (Fig. 3.11) is also reduced. Some lead inductance will remain, which cannot be removed. The most widely used board level retrofit capacitors are known as Micro-Q™.[2] Other manufacturers provide similar products. An example of this type of capacitor is detailed in Fig. 3.13. This device exists only in pin grid array (PGA) or Dual-In-Line (DIP) packaging. For PGA applications, unique assemblies are available based on the particular pinout and power/ground pin arrangements.

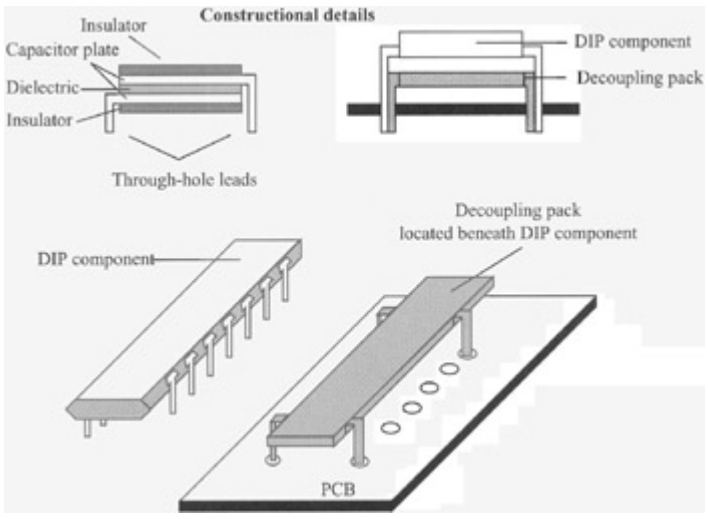

Figure 3.13: Retrofit decoupling capacitor—DIP mounting style.

A retrofit capacitor has a self-resonant frequency generally in the range of 10 to 50 MHz, depending on the capacitance value of the device. Since DIP style leads are provided, higher frequency use cannot occur owing to excessive lead inductance. Although sometimes termed a "retrofit" device, the improved decoupling performance of these capacitors, compared to that of axial leaded capacitors on two-layer boards, makes them suitable only for initial design implementation.

Poor planning during PCB layout and component selection may require use of Micro-Q. As yet, no equivalent retrofit for SMT components is available.

Placement of 1-nF (1000 pF) capacitors (capacitors with a very high self-resonant frequency) on a 1-in. (2.54 cm) grid may provide additional protection from RF currents for both signal traces and power planes, especially if a high-density PCB stackup is provided [6]. A lumped model analysis of the PCB shows that the capacitors will still function as desired, regardless of where the device is actually placed for overall decoupling performance. Depending on the resonant structure of the board, values of the capacitors placed in the grid may be as small as 30–40 pF [7, 8].

VLSI and high-speed components (F, ACT, BCT, CMOS, ECL, etc.) may require additional use of parallel decoupling. As slew rates of components become faster, a greater spectral distribution of RF energy is developed. Parallel capacitors generally provide optimal bypassing of power plane noise. Multiple paired sets of capacitors are placed between the power and ground pins of VLSI components located around all four sides. These high-frequency decoupling capacitors are typically rated 0.1 µF in parallel with 0.001 µF for 50 MHz systems. Higher clock frequencies generally require use of a parallel combination of 0.01 µF and 100 pF components. (The uses of parallel capacitors were discussed in Section 3.3.)

Although there has been considerable debate among engineers on how to install decoupling capacitors, the one that provides optimal performance must be chosen, application dependent. One implementation technique is to run a trace from the capacitor to the device and then use a via to connect the trace to the power and ground planes. Another technique is to run separate vias to the planes from both capacitor and component, letting the current flow through a very low-inductance plane between the two devices. Various combinations of this layout technique are presented in Fig. 3.14 [7, 8].

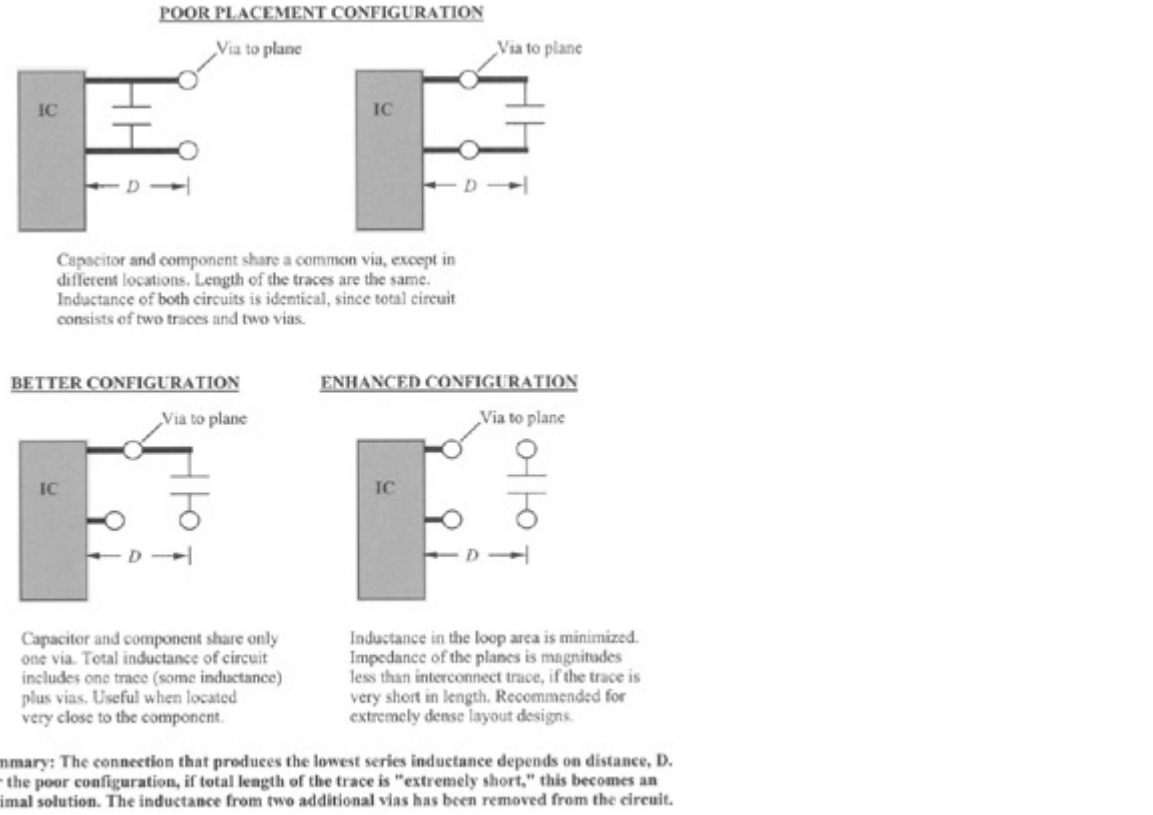
POOR PLACEMENT CONFIGURATION
Via to plane
IC
D
Via to plane
IC
D
Capacitor and component share a common via, except in different locations. Length of the traces are the same. Inductance of both circuits is identical, since total circuit consists of two traces and two vias.
BETTER CONFIGURATION
Via to plane
IC
D
Capacitor and component share only one via. Total inductance of circuit includes one trace (some inductance) plus vias. Useful when located very close to the component.
ENHANCED CONFIGURATION
Via to plane
IC
D
Inductance in the loop area is minimized. Impedance of the planes is magnitudes less than interconnect trace, if the trace is very short in length. Recommended for extremely dense layout designs.
Summary: The connection that produces the lowest series inductance depends on distance, D. For the poor configuration, if total length of the trace is "extremely short," this becomes an optimal solution. The inductance from two additional vias has been removed from the circuit.

Figure 3.14: Various mounting methodologies.

For the first technique, running a trace from capacitor to a component, and then connecting the composite configuration to the power and ground planes by a vias, is a poor implementation technique, even if the trace is physically wide, regardless of location. The reason this is a poor implementation technique deals with loop area and trace inductance. The loop area of the current path between the circuit to one of the planes, through a via, plus the trace distance through the capacitor back through another trace and via to the other plane, is physically much larger than the loop area dimension that is commonly assumed. Total inductance of the loop area is also very large.

Why do we care about the loop area? Because the bigger the loop, the more flux that is observed as EMI owing to the higher the inductance. With inductance, there exists a lower self-resonant frequency among other items. These other items make the antiresonant frequency of the capacitor higher, thus lowering the bandwidth of performance. With a low-bandwidth performance, use of more discrete capacitors to achieve the same bypass effectiveness is required. The goal is to create a low-impedance network over a large spectral area for the power distribution system. Therefore, component power pins must be routed directly to the power and ground planes. In addition, the decoupling capacitor must be connected directly to the planes to minimize the current loop area and trace/via inductance [8].

In addition, current passes mostly through the decoupling capacitor immediately adjacent to the integrated circuits. The impedance of the capacitor is finite. Some of the current is fed back through the supply planes, distributing it around the circuit. This loop may develop a noise voltage of magnitude $V = IZ$, where Z is the impedance of the power supply. Although this impedance is low, it is still significant, and it is largely inductive at higher frequencies.

3.5.4 Single- and Double-Sided Assemblies

While the focus in this chapter is on multilayer boards, single- and double-sided assemblies also require decoupling. Figure 3.15 illustrates ways of locating a decoupling capacitor for a single- or double-sided design.

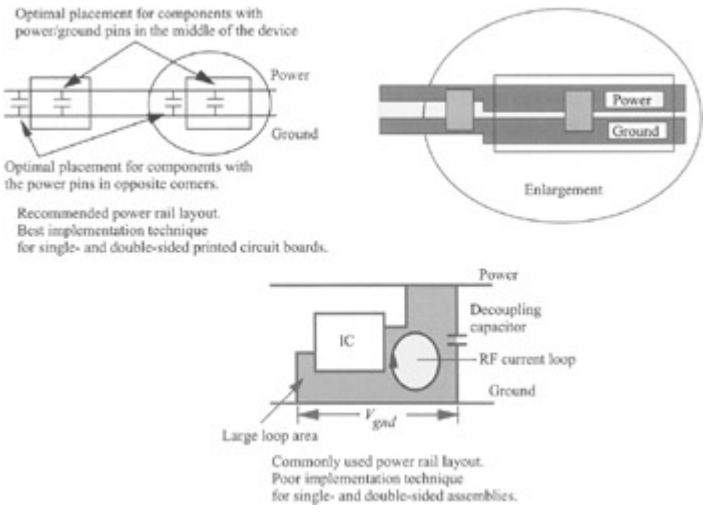

Figure 3.15: Placement of decoupling capacitors, single- and double-sided board.

In Fig. 3.15, V_{gnd} is *LdI/dt*-induced noise in the ground trace flowing in the decoupling capacitor loop. This V_{gnd} drives the ground structure of the board, contributing to the development of common-mode voltage levels. One must minimize the ground path impedance between decoupling capacitors.

3.5.5 Mounting Pads

Where very high-frequency performance is required, multiple vias and short fat traces reduce overall inductance of the interconnect. Using an increased size of SMT pad with multiple vias to the reference plane makes a significant improvement in high-frequency performance. If the via is placed internal to the mounting pad, additional benefit is achieved (Fig. 3.16, Best Configuration).

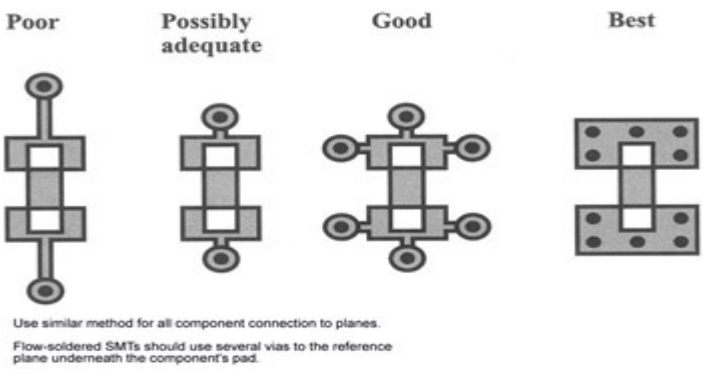
Poor
Possibly adequate
Good
Best
Use similar method for all component connection to planes.
Flow-soldered SMTs should use several vias to the reference plane underneath the component's pad.

Figure 3.16: Comparison of connection methods for SMT components.

Using analysis tools, we see that calculated inductance for the following are on the order of

- Pair of surface traces — 10–15 nH/inch
- Pair of vias for decoupling capacitor — 0.40–1 nH (200–500 pH each)
- Plane inductance — 0.1 nH

These numbers indicate that trace and via inductance is significantly greater than planar inductance.

Maximizing the physical width of the connection from the capacitor to planes minimizes total loop inductance. The wider the trace, the lower the inductance. The same goes for connecting component pads to planes. For each additional via (multiple vias in a pad), inductance will be reduced, similar in concept to resistors placed in parallel. For connections between locations through a reference plane, there is very low inductance. The capacitance between the power and ground planes can also be very useful for decoupling when placed physically close together. For example, if power and ground are placed adjacent to each other in the middle of a 0.062 in. (1.6 mm) thick board, an additional 0.062-in. trace length is present from the top layer to the power plane and back up to the top layer from the ground plane, often through a single via at both ends. This via has a significant amount of inductance that will be added to the total inductance

of the loop.

For a +5V/+3.3V system, planes can be located close to the outer side of the PCB and decoupled from the side closest to the pair. Remember that a decoupling capacitor also provides a path for return current to travel through the board within the plane. Driving a rising-edge transition means that return current has to get back to the power pin of the driver. Another reason for locating traces between a pair of *ground planes* is that ground vias or bypass capacitors are not required to provide a path for RF return currents. To review, bypassing allows energy to be transferred from one location to another at the same potential, while decoupling is between planes of different potential. Optimal placement of capacitors minimizes the RF return path. The important item to remember is not the specific numeric value of capacitance, or total inductance, but the *magnitude* of impedance, which must be extremely low for optimal performance.

Figure 3.17 illustrates various patterns to minimize trace inductance and enhance the performance of decoupling capacitors for multilayer designs. Use of very small SMT components may not allow placement of vias between the mounting pads; thus, use of vias on the inside edge becomes mandatory.

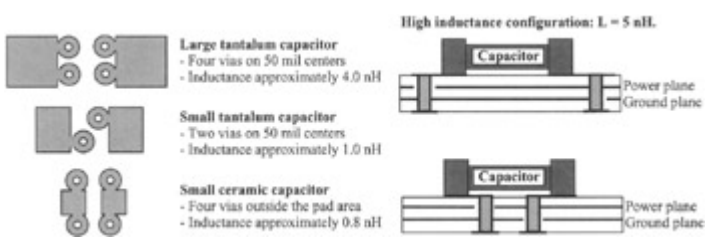

Figure 3.17: Capacitor placement patterns for optimal performance-multilayer implementation.

Regardless of whether the PCB is simple or complex, almost all products require a trace to be present between a component lead and capacitor, or interconnect via. This interconnect trace, also identified as pin-escape, breakout, and similar terminology, exists by virtue of the fact that component pins are spaced tightly together with small packaging densities. A trace must be routed from the component to a via located nearby for connection to a signal, power, or ground plane. It is not possible, manufacturing wise, to have large vias embedded in a component's mounting pad. Solder may flow into the via, preventing the component from having a secure bond connection in addition to other manufacturing concerns. Figure 3.18 illustrates layout techniques with comments.

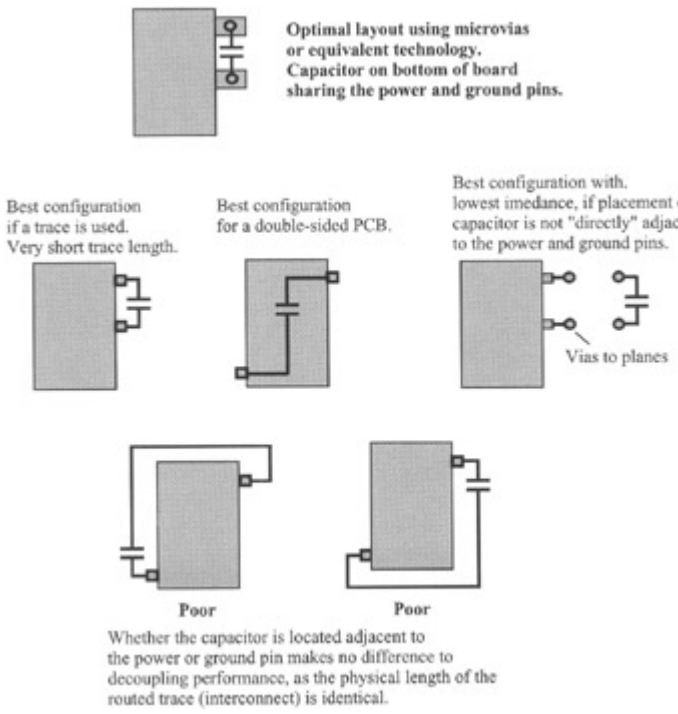
Optimal layout using microvias
or equivalent technology.
Capacitor on bottom of board
sharing the power and ground pins.
Best configuration
if a trace is used.
Very short trace length.
Best configuration
for a double-sided PCB.
Best configuration with.
lowest imedance, if placement of
capacitor is not "directly" adjacent
to the power and ground pins.
Vias to planes
Poor
Poor
Whether the capacitor is located adjacent to
the power or ground pin makes no difference to
decoupling performance, as the physical length of the
routed trace (interconnect) is identical.

Figure 3.18: Capacitor placement recommendation.

3.5.6 Microvias

A technology known as microvias permits use of vias embedded within component mounting pads. These microvias minimize the amount of solder absorbed by the via during a wave or IR soldering process. Additional costs may be incurred from use of this technology, which is becoming common in extremely high-density, high-performance designs. One advantage of using microvias is to minimize trace inductance between the mounting pad and a remote via. In addition, less real estate is required for

incorporation of the microvia, thus allowing greater routing densities to exist. If more traces can be routed within internal layers, fewer routing planes may be required. The use of fewer planes may be more cost effective then implementing the cost of microvia technology.

[2]Micro-Q™ is a trademark of Circuit Components Inc. (formerly Rogers Corporation).

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Chapter 3 - Bypassing and Decoupling

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

IEEE Press © 2000

Recommend this title? yes no

3.6 HOW TO PROPERLY SELECT A CAPACITOR

3.6.1 Bypass and Decoupling

Components with periodic switching states must be given emphasis to be RF decoupled. This emphasis is due to switching energy injected into the power and ground distribution system. This energy will be transferred to other circuits or subsections as common-mode or differential-mode RF energy. Bulk capacitors, such as tantalum and high-frequency ceramic monolithic are both required, each for a different application. Furthermore, monolithic capacitors must have a self-resonant frequency higher than the clock harmonics or the switching frequency requiring suppression. Typically, one selects a capacitor with a self-resonant frequency in the range of 10–30 MHz for circuits with edge rates of 2 ns or less. Many PCBs are self-resonant in the 200–400 MHz range. Proper selection of decoupling capacitors, along with the self-resonant frequency of the PCB structure (acting as one large capacitor), will provide enhanced EMI suppression. Tables 3.2 and 3.3 (see Section 3.2.4) are useful for axial or radial lead capacitors. Surface mount devices have a higher self-resonant frequency by approximately two orders of magnitude (or 100x) as a result of less lead inductance. Aluminum electrolytic capacitors are ineffective for high-frequency decoupling and are best suited for power supply subsystems or power line filtering.

It is common to select a decoupling capacitor for a particular application, usually the first harmonic of a clock or processor. A capacitor is sometimes selected for the third or fifth harmonic, since this is where a majority of RF current is observed. There also needs to be plenty of larger discrete capacitors that are application dependent: bulk and decoupling. The use of common decoupling capacitor value of 0.1 µF can be too inductive and too slow to supply charge current at frequencies above 50 MHz.

Use of 0.1 µF capacitors is common in many products. When asking a designer why they use this value, the answer most frequently qiven is "that is the way it has always been, and the designer before them used this value capacitor." No thought or analysis is considered why this value was used or selected. Although a manufacturer's data sheet indicates use of common values (e.g., 0.1 µF), what assurance does one have that the technical writer was provided the results of analysis from electrical designers that was accurate? In addition, did the person responsible for documentation investigate and question concerns detailed within this chapter? Many technical writers use information from a prior job, without justification, if this information is valid for the document being developed.

For historical purposes, in 1965, the United States Air Force discovered that if it decoupled airborne electronic equipment, the plane would be able to communicate by radio. Use of 0.1 µF electrolytic capacitors was incorporated with long wire leads (large ESL and ESR values). The operating frequency of the equipment was 200 kHz. Consequently, if 0.1 µF is acceptable for 200 kHz systems, then it must be acceptable for 200 MHz products, which is totally wrong! The key to optimal performance is to calculate the capacitor for functionality reasons. A capacitor should not be used based on historical usage without understanding how and why a particular value was chosen.

It is alleged that designers choose decade values of capacitor (0.1, 0.01, 0.001 µF, 100 pF) units that exclusively have zeros (0's) and ones (1's), because "digital" engineers think binary.

When performing component placement on a PCB, one should make physical provisions for adequate high-frequency RF decoupling. One should also verify that all bypass and decoupling capacitors chosen are selected based on intended application. This is especially true for clock generation circuits. The self-resonant frequency must take into account all significant clock harmonics requiring suppression, which is generally considered the fifth harmonic of the original clock frequency. Capacitive reactance (self-resonant reactance in ohms) is calculated as

(3.7)
$$X_c = \frac{1}{2\pi f C}$$

Get MathML

where X_c = capacitance reactance (ohms)
f = resonant frequency (hertz)
C = capacitance value (farads)

The minimum capacitive value of the bypass capacitor required for optimal performance is determined by the maximum amount of voltage drop allowable across the capacitor as a result of a transient current surge. This voltage drop is exacerbated when a component operates under maximum capacitive load. An appropriate value for bypassing can be easily calculated by

(3.8)
$$C = \frac{I\Delta t}{\Delta V} \text{ (farads)}$$

Get MathML

where C = capacitance value
Δt = duration of the transient event
ΔV = allowable voltage drop

For example, a typical 74HC component has an input transient surge of 20 mA for 10 ns. The voltage drop must be less than 100 mV to ensure proper logic transitions. The optimal value for the capacitor is

$$C = \frac{(20\text{ mA})(10\text{ ns})}{(100\text{ mV})} = 2\text{ nF or }0.002\text{ uF}$$

Get MathML

A problem with using these equations as written lies with lead inductance in the decoupling loop. Additional voltage spiking occurs across the inductance. For any magnitude of noise spike, the maximum amount of series inductance is described by

(3.9)
$$L = \frac{V\Delta t}{\Delta I} \text{ (henries)}$$

Get MathML

where L = inductance value
V = maximum noise spike
Δt = duration of the transient event

ΔI = transient current in the decoupling loop

For this same component, with a transient surge of 20 mA and an edge rate (rise/fall time) of 2 ns, the inductive values that restrict a noise spike to 100 mV peak is

$$L = \frac{(100\ \text{mV})(2\ \text{ns})}{(20\ \text{mA})} = 10\ \text{nH}$$

➪ Get MathML

This means that total lead and series inductance cannot exceed 10 nH. Referring back to Fig. 3.14, we see that total ESL of the circuit must be kept below 10 nH; this is a challenging task when traces are required to be routed between component and capacitor. One should not forget to include the inductance associated with the bond wires internal to a component package.

3.6.2 Capacitive Effects on Signal Traces

Capacitors can be used to shape differential-mode signals on individual traces. These capacitors are generally found in I/O circuits and are rarely used in clock networks. The capacitor, *C*, alters the signal edge (slew rate) by rounding the time period that the signal edge transition takes to change from logic state 0 to logic state 1. This is illustrated in Fig. 3.19.

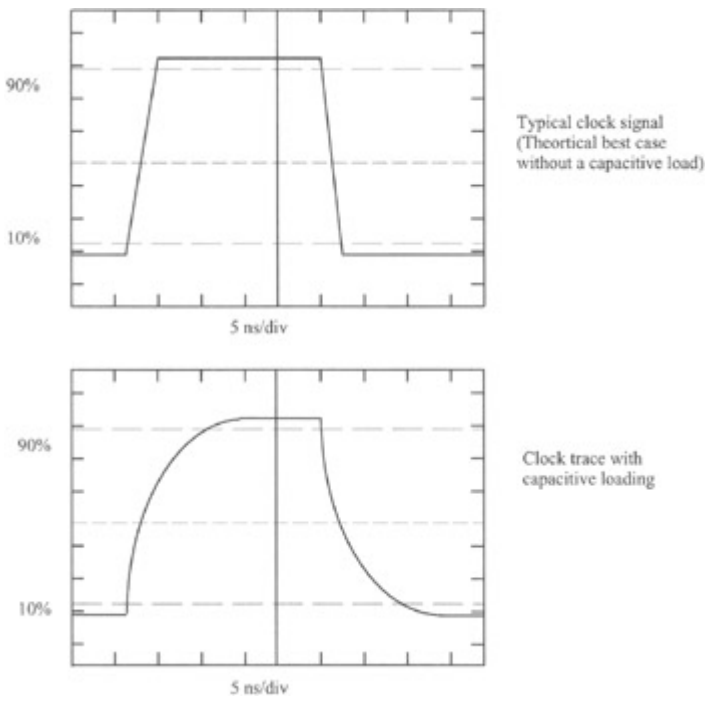


Figure 3.19: Capacitive effects on clock signals.

Figure 3.19 shows the change in the slew rate (clock edge) of the desired signal. Although the transition points remain unchanged, the time period, t_r, is different. This elongation, or slowing of the signal edge, is a result of the capacitor charging and discharging. The change in transition time is described by the equations and illustration of Fig. 3.20. Note that a Thevenin equivalent circuit is shown, without the load. The source voltage, V_b, and series impedance, R_s, are internal to the driver or clock generation circuit. The capacitive effect on the trace is a result of this capacitor being located in the circuit. To determine the time rate of change of the capacitor of Fig. 3.19, the equations in Fig. 3.20 are used.

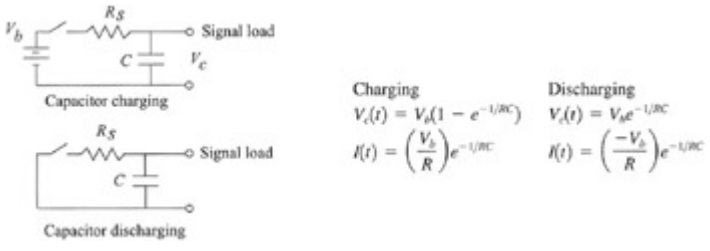


Figure 3.20: Capacitor equations, charging and discharging.

When a Fourier analysis is performed on this signal edge transition (conversion from time to frequency domain), a significant reduction of RF energy occurs, along with a decrease in spectral RF distribution. Hence,

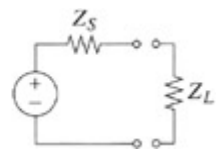
we see improved EMI compliance. Caution is required during the design stage to ensure that slower edge rates will not adversely affect operational performance.

The value used to alter the shape of a signal can be calculated in two ways. Although capacitance is calculated for optimal performance at a particular resonant frequency, use and implementation depend on installation, lead-length inductance, trace length inductance, and other parasitic parameters that may change the resonant frequency of the capacitor. The installed value of capacitive reactance is the item of interest. Calculating the value of capacitance will be in the ballpark and is generally accurate enough for actual implementation.

Before calculating a filter capacitor value to waveshape a signal, the Thevenin impedance of the network must be determined. The impedance should be equal to two resistors placed in parallel. For example, using a Thevenin equivalent circuit Eq. (3.10), assume Z_s = 150 Ω and Z_L = 2.0 k Ω where Z_s is source impedance and Z_L is load.

(3.10)

$$Z_t = \frac{Z_s * Z_L}{Z_s + Z_L} = \frac{150 * 2000}{2150} = 140\Omega$$



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Method 1

Equation (3.11) is used to determine the maximum capacitance value for wave shaping, based on knowing the edge rate of the clock signal.

(3.11)

$$tr = k\,R_t\,C_{\max} = 3.3 * R_t * C_{\max}$$

$$C_{\max} = \frac{0.3\ t_r}{R_t}$$

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where

t_r	=	edge rate of the signal (the faster of either the rising or falling edge)
k	=	one time constant
R_t	=	total resistance within the network
$C_{\max}$	=	maximum capacitance value to be used

Note *C* in nanofarads if t_r is in nanoseconds

C in picofarads if t_r is in picoseconds

The capacitor must be chosen so that the edge transition time (t_r = 3.3*R* * *C*) equals an acceptable rise or fall time for proper functionality of the signal; otherwise baseline shift may occur. Baseline shift refers to the steady-state voltage level that is identified as logic LOW or logic HIGH for a particular logic family. The number 3.3 is the value of the time constant for a capacitor to charge, based on the time constant equation τ = *RC*. Approximately three (3) time constants equal one (1) rise time. Since we are interested in only one time constant for calculating this capacitance value, the value of the time constant period, $k = 1/3t_r$, which becomes $3.3t_r$ when incorporated within the equation (inverse of $1/3t_r$).

For example, if the edge rate is 5 ns and the impedance of the circuit is 140 Ω, calculate the maximum value of *C* as

(3.12)

$$C_{\max} = \frac{0.3 * 5}{140} = 0.01\ \text{nF}\ \text{ or }\ 10\ \text{pF}$$

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A 60-MHz clock with a period of 8.33 ns on and 8.33 ns off, R = 33 Ω (typical for an unterminated TTL part) has an acceptable $t_r = t_f$ = 2 ns (25% of the on or off value). Therefore,

(3.13) $$\left(C = \frac{0.3 * t_r}{R_t}\right) \quad C = \frac{0.3\,(2 * 10^{-9})}{33} = 18\ \text{pF}$$

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Method 2

- For wave shaping, determine the highest frequency to be filtered, f_{max}.
- For differential pair traces, determine the maximum tolerable value for each capacitor. To minimize signal distortion, using Eq. (3.14)

(3.14) $$C_{max} = \frac{100}{f_{max} * R_t}$$

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where C is in nanofarads, f in MHz, and R in ohms.

To filter a 20 MHz signal with R_L = 140 Ω, the capacitance value with low source impedance, Z_c, would be

(3.15) $$C_{min} = \frac{100}{20 * 140} = 0.036\ \text{nF or } 36\ \text{pF}$$

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When using capacitors to alter the characteristics of a signal transition, implement the following:

- If degradation of the edge rate is acceptable, generally up to three times the value of calculated C_{max}, increase the capacitance value to the next highest standard value.
- Select a capacitor with proper voltage rating and dielectric material for intended use.
- Select a capacitor with a tight tolerance level. A tolerance level of +80/-0% is acceptable for power supply filtering but is inappropriate for high-speed signals.
- Install the capacitor with minimal lead- and trace inductance.
- Verify the functionality of the circuit with the capacitor installed. Too large a value capacitor can cause excessive signal degradation.

3.6.3 Bulk

Bulk capacitors ensure that a sufficient amount of DC voltage and current is available, especially when digital components transition all data, address, and control signals simultaneously under maximum capacitive load. Maximum capacitive load refers to the total amount of current that must enter the power pins of a component. The component then sends this transient current to all output loads. Each load connected to a routed net consumes current. The greater the number of loads, the greater the amount of current that must pass through the source driver.

Components switching logic states can cause current fluctuations on power and ground planes. These fluctuations affect the performance of other components owing to voltage sags. Bulk capacitors thus provide energy storage for circuits to maintain optimal voltage and current requirements.

Bulk capacitors (tantalum dielectric) are required, in addition to higher self-resonant frequency decoupling, to provide DC power for components,

minimizing RF modulation in the power distribution network. One bulk capacitor should be located for every two LSI and VLSI components, in addition to the following locations:

- Power entry connectors from the power supply.
- Power terminals on interconnnects for daughter cards, peripheral devices, and secondary circuits.
- Near power-consuming digital components.
- The furthest location from the input power connector.
- High-density component placement remote from the DC input power connector.
- Adjacent to clock generation circuits.

When using bulk capacitors, the voltage rating can be calculated such that the nominal voltage level equals 50% of the capacitor's actual rating to prevent self-destruction, should a voltage surge occur. For example, with power at 5 volts, one should use a capacitor with a minimum of a 10-volt rating.

Memory arrays require additional bulk capacitors owing to the extra current required for proper operation during a refresh cycle. The same is true for VLSI components with large pin counts. High-density pin grid array (PGA) modules also must have additional bulk capacitors provided, especially when all signal, address, and control pins switch simultaneously under maximum capacitive load.

Equation (3.4)—see Section 3.2.3—can be modified to calculate the peak surge current consumed by all capacitors. It is noted that more is not necessarily better. An excessive number of capacitors can draw a large amount of current, thereby placing a strain on the power supply.

Selection of a capacitor for a particular application, based on past experience with slow speed digital logic, will generally not provide optimal bypassing and decoupling when used with high-technology, high-speed designs. Considerations of resonance, placement on the PCB, lead-length inductance, existence of power and ground planes, and the like must all be included when selecting a capacitor or capacitor combination.

For bulk capacitors, the following procedures are provided to determine optimal selection [9]:

Example 1

1. Determine maximum current (ΔI) consumption anticipated on the board. Assume all gates switch simultaneously. Include the effect of power surges by logic crossover (cross-conduction currents).
2. Calculate the maximum amount of power supply noise permitted (ΔV) by devices for functionality purposes. Factor in a safety margin.
3. Determine maximum common-path impedance acceptable to the circuit.

(3.16) $$Z_{cm} = \Delta V / \Delta I$$

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4. If solid planes are used, allocate the impedance, Z_{cm}, to the connection between the power and ground structure.
5. Calculate the impedance of the interconnect cable, Z_{cable} ($=j2\pi fL_{cable}$), from the power supply to the PCB. Add this value to Z_{cm} to determine the frequency below which the power supply wiring is adequate ($Z_{total} = Z_{cm} + L_{cable}$).

(3.17)

$$f = \frac{Z_{\text{total}}}{2\,\pi\,Z_{\text{cable}}}$$

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6. If the switching frequency is below the calculated *f* of Eq. (3.17), the power supply wiring is fine. Above *f*, bulk capacitors, C_{bulk}, are required. Calculate the value of the bulk capacitor for an impedance value Z_{total} at frequency *f*.

(3.18)
$$C_{\text{bulk}} = \frac{1}{2\,\pi\,f\,Z_{\text{total}}}$$

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Example 2

A PCB has 200 CMOS gates (*G*), each switching 5 *pF* (*C*) loads within a 2-ns time period. Power supply inductance is 80 nH.

(3.19)
$$\Delta I = GC\frac{\Delta V}{\Delta t} = 200(5\ pF)\frac{5V}{2\ \text{ns}} = 2.5\ \text{A (worst-case peak surge)}$$

$$\Delta V = 0.200\ \text{V (from noise margin budget)}$$

$$Z_{\text{total}} = \frac{\Delta V}{\Delta I} = \frac{0.20}{2.5} = 0.08\ \Omega$$

$$L_{\text{cable}} = 80\ \text{nH}$$

$$f_{ps} = \frac{Z_{\text{total}}}{2\,\pi\,L_{\text{cable}}} = \frac{0.08\ \Omega}{2\,\pi\ 80\ \text{nH}} = 159\ \text{kHz}$$

$$C = \frac{1}{2\,\pi\,f_{ps}\,Z_{\text{total}}} = 12.5\ \mu\text{F}$$

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Capacitors commonly found on PCBs for bulk purposes are generally in the range of 4.7–100 µF.

Chapter 3 - Bypassing and Decoupling

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

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Chapter 4: Clock Circuits, Trace Routing, and Terminations

4.1 CREATING TRANSMISSION LINES WITHIN A PCB

With today's high-technology products and faster logic devices, transmission line effects have become a limiting factor for proper circuit operation. Traces routed adjacent to a reference plane, or RF return path, form a simple transmission line. Consider the case of a multi-layer PCB. When a trace is routed on an outer layer, we have the microstrip topology, though it may be asymmetrical in construction. When a trace is routed on an internal layer, this is called the *stripline*. This chapter provides details, definitions, and differences regarding microstrip and stripline topology.

Two basic topologies are available for developing a transmission line structure within a PCB. Each topology has several configurations: microstrip (single and embedded) and stripline (single, dual, symmetrical, or asymmetrical). Another topology, co-planar, can be implemented in both microstrip and stripline configuration.

Logic families have different characteristic source impedance. For example, emitter-coupled logic (ECL) has a source and load impedance of 50 Ω. Transistor-transistor logic (TTL) has a source impedance range of 20–100 Ω and a load impedance that is magnitudes higher. If a transmission line is to be created within a PCB, the engineer must seek to match both the source and load impedance of the logic family being used within a circuit design.

Most high-speed traces must be impedance controlled. Calculations to determine optimal trace width and distance to the nearest reference plane must occur prior to board layout. Board manufacturers and CAD programs can easily perform these calculations. These calculations can also be downloaded from the World Wide Web for free. If necessary, board fabricators can be consulted for assistance in designing the assembly, or a computer application program can be used to determine the most effective approach relative to trace width and distance spacing between planes for optimal performance.

The approximate formulas that calculate the impedance of a transmission line may not be fully accurate owing to manufacturing tolerances that occur during the fabrication process. These formulas were simplified from exact models. Stock material may have a different thickness and dielectric constant value. The finished etched trace width may be different from a desired design requirement, or any number of manufacturing concerns may be present. The board vendors know the accurate numeric variables to be used in the impedance equations. These vendors need to be consulted when the need for extreme accuracy is required, using real or actual dielectric constant values, as well as the finished etched trace width for both base and crest dimensions, detailed in Fig. 4.1.

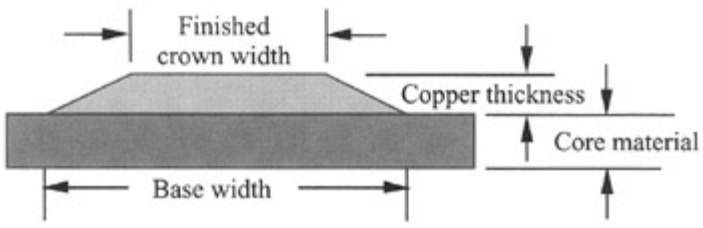

Figure 4.1: Finished trace width dimensions after etching.

There are several effects in determining the accuracy of impedance for transmission lines. First-order effects include line width, height above a reference plane (dielectric thickness), and dielectric constant. These effects deal with basic dimensions used within the formulas presented herein to define trace impedance. Second-order effects that may alter trace impedance include

- Extent of the return path.
- Trace thickness.
- Side wall shape.
- Solder mask coverage.
- Use of mixed dielectrics within the same assembly.

First-order effects are detailed in the equations for microstrip and stripline topologies. Use of field solvers (which are beyond the scope of this book) reveals that second-order effects result in

1. *Extent of the return path*. The longer the trace route, the greater the inductance value. This distance also includes the RF return path.

2. *Trace thickness*. A change in trace thickness will alter trace impedance at approximately 2 ohms/mil when using 1/2-oz. to 1-oz. copper.

3. *Side wall shape*. Based on Fig. 4.1, a change in sidewall dimensions will cause less than a 1% change in trace impedance. The sensitivity of this impedance change is 2 ohms/mil. With typical etch back at 0.25 mils, this tolerance change is approximately 0.5 ohms.

4. *Solder mask coverage*. Using a standard thickness of soldermask, we find that the sensitivity of change is approximately 3 ohms/mil (6 %/mil). Change the impedance value of microstrip traces by this amount when soldermask is provided.

5. *Use of mixed dielectrics within the same assembly*. Certain assemblies will contain material with different types of dielectric constants. In order to determine the effects of a mixed dielectric assembly on overall impedance, use of field solvers (sophisticated software) is required.

Sensitivity analysis, either manual or simulated, allows one to determine manufacturing tolerances, if the design is critical relative to certain design features or impedance control. The high and low ends of each parameter should be examined, taking into consideration both first- and second-order effects.

Approximations should be used only for tradeoff analysis when using first-order effects. Rules-of-thumb are powerful tools allowing one to perform quick sanity checks. The accuracy of analytical approximations varies, depending on specific applications, and is hard to generate. Accuracy of simulation tools is based on models. The models for the circuit may not be available. Before relying on simulation tools to calculate trace impedance, the vendor of the PCB should be consulted to verify the accuracy of parameters used within the equations. Without accurate numbers for material proprieties, a lot of time will be wasted trying to simulate an answer, when a simple calculator will provide a result that is accurate for most applications.

Note None of the equations provided in the next section for microstrip and stripline is applicable to PCBs constructed of two or more dielectric materials, excluding air, or fabricated with more than one

type of laminate. All equations are extracted from *IPC-D-317A*, *Design Guidelines for Electronic Packaging Utilizing High-Speed Technique*[1] [4].

[1]Within the IPC standardsm typographical and mathematical errors exist in the section related to impedance calculation. Before applying equations detailed within IPC-D-317, study and identify all errors before literal use. Equations presented herein have been independently verified for accuracy.

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4.2 TOPOLOGY CONFIGURATIONS

4.2.1 Microstrip Topology

Microstrip is one topology used to provide trace-controlled impedance on a PCB for digital circuits. Microstrip lines are exposed to both air and a dielectric referenced to a planar structure. The approximate formula for calculating the impedance of a surface microstrip trace is provided in Eq. (4.1) for the configuration of Fig 4.2. The intrinsic capacitance of the trace is described by Eq. (4.2).

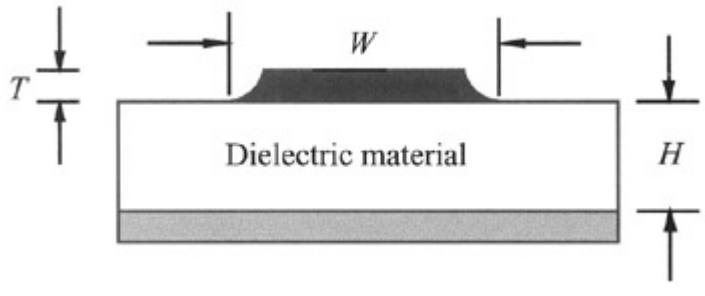

Figure 4.2: Surface microstrip topology.

(4.1) $$Z_o = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}}\right) ln\left(\frac{5.98\,H}{0.8\,W + T}\right) \Omega \quad \text{Valid for } 15 < W < 25 \text{ mils}$$

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(4.2) $$Z_o = \left(\frac{79}{\sqrt{\varepsilon_r + 1.41}}\right) ln\left(\frac{5.98\,H}{0.8\,W + T}\right) \Omega \quad \text{Valid for } 5 < W < 15 \text{ mils}$$

$$C_O = \frac{0.67(\varepsilon_r + 1.41)}{ln\left(\frac{5.98H}{0.8W + T}\right)} \quad \text{pf/in.}$$

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where
Z_o = characteristic impedance (ohms)
W = width of the trace
T = thickness of the trace
H = distance between signal trace and reference plane
C_o = intrinsic capacitance of the trace (pF/unit distance)
ϵ_r = dielectric constant of the planar material

Note Use consistent dimensions for width, thickness, and height above a reference plane (inches or centimeters). The value for C_o is provided in inches, which is easily converted to metric.

Equation (4.1) is typically accurate to ± 5% when the ratio of *W* to *H* is 0.6 or less. When the ratio of *W* to *H* is between 0.6 and 2.0, accuracy drops to ± 20%.

When measuring or calculating trace impedance, the width of the line should technically be measured at the middle of the trace thickness. Depending on the manufacturing process, the finished line width after etching may be different from that specified by Fig. 4.2. The width of the

copper on the top of the trace (crown dimension) may be etched away, making the trace width smaller than desired. Using the average between top and bottom of the trace thickness, we find that a more typical, accurate impedance number is possible. With respect to the measurement of a trace's width, with a *ln* (natural logarithm) expression, how much significance should we give to achieving a highly accurate trace impedance value for the majority of designs? Most manufacturing tolerances are well within 10% of desired impedance. The magnitude of the impedance change, based on where we measure trace thickness, is so small that it can be ignored for practically all designs below 1 GHz.

The propagation delay of a signal routed microstrip is described by Eq. (4.3). This equation has as a variable only ϵ_r, or the value of the dielectric constant. This equation states that the propagational speed of a signal within this transmission line is related only to the effective permittivity of the dielectric material [2].

(4.3)
$$t_{pd} = 1.017\sqrt{0.475\,\varepsilon_r + 0.67} \quad \text{(ns/ft)}$$
or
$$t_{pd} = 85\sqrt{0.475\,\varepsilon_r + 0.67} \quad \text{(ps/in.)}$$

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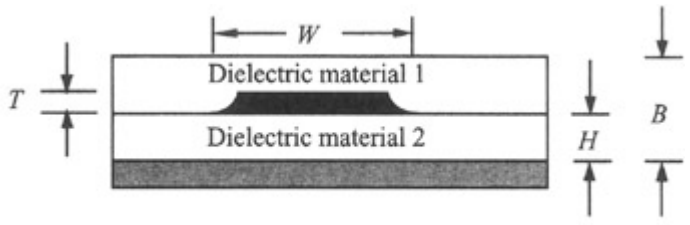
4.2.2 Embedded Microstrip Topology

The embedded microstrip is a modified version of a standard microstrip. The difference lies in providing a dielectric material on the top surface of the copper trace. This dielectric may include another routing layer such as core, soldermask, conformal coating, potting, or other material required for functional or mechanical purposes. As long as the material provided contains the same dielectric constant, with a thickness of 0.008 to 0.010 in. (0.0020 mm to 0.0025 mm), air or the environment will have little effect on the impedance value. Another way to view the embedded microstrip is to compare it to a single, asymmetric stripline with one plane infinitely far away.

Coated microstrip uses the same conductor geometry as uncoated, except that the effective relative permittivity will be higher. Coated microstrip refers to placing a substrate on the outer microstrip layer. The dielectric on top of the trace may be asymmetrical to the host material. The difference between coated and uncoated microstrip is that the conductors on the top layer are fully enclosed by a dielectric substrate. The equations for embedded microstrip are the same as those for uncoated, except, with a modified permittivity, ϵ'_r. If the dielectric thickness above the conductor is more than a few thousandths of an inch, ϵ'_r will need to be determined through either experimentation or use of an electromagnetic field solver. For "very thin" coatings, such as soldermask or conformal coating, the effect is minimal. Masks and coatings will drop the impedance of the trace by 0.5 to 1.0 ohm for every 1 mil (0.001 in. or 0.025 mm) of material located on top of the trace.

The approximate characteristic impedance formula for embedded microstrip is provided by Eq. (4.4). For embedded microstrip, particularly those with asymmetrical dielectric heights, knowledge of the base and crown widths after etching will improve accuracy. These formulas are reasonable as long as the thickness of the upper dielectric material [$B - (T + H)$] is less than 0.002 in. (0.05 mm). If the coating is thicker, or if the relative dielectric coefficient of the coating is different (e.g., conformal coating), the impedance will typically be somewhere between those calculated between microstrip and embedded microstrip.

The characteristic impedance of embedded microstrip is shown in Eq. (4.4) for the configuration shown in Fig. 4.3. The intrinsic capacitance of the trace is defined by Eq. (4.5).



Note: Thickness of the dielectric material may be asymmetrical.

Figure 4.3: Embedded microstrip topology.

(4.4)

$$Z_o = \left(\frac{87}{\sqrt{\varepsilon' + 1.41}}\right) ln \left(\frac{5.98\,H}{0.8\,W + T}\right) \Omega$$

where $\varepsilon'_r = \varepsilon_r\{1 - e^{\left(\frac{-1.55B}{H}\right)}\}$

➡ Get MathML

(4.5)

$$C_o = \frac{1.41(\varepsilon'_r)}{\ln\left(\frac{5.98\,H}{0.8\,W + T}\right)} \text{ pF/in.}$$

➡ Get MathML

where
- Z_o = characteristic impedance (ohms)
- C_o = intrinsic capacitance of the trace (pF/unit distance)
- W = width of the trace
- T = thickness of the trace
- H = distance between signal trace and reference plane
- B = overall distance of both dielectrics
- ϵ_r = dielectric constant of the planar material
- $0.1 < W/H < 3.0$
- $0.1 < \epsilon_r < 15$

Note Use consistent dimensions for width, thickness, and distance spacing between layers (inches or centimeters). The value for C_o is provided in inches, which is easily converted to metric.

The propagation delay of a signal-routed embedded microstrip is provided by Eq. (4.6). For a typical embedded microstrip, with FR-4 core material and a dielectric constant of 4.1, propagation delay is 0.35 ns/cm or 1.65 ns/ft (0.137 ns/in.). This propagation delay equation is nearly the same as single stripline, discussed next, except with a modified ϵ'_r.

(4.6)

$$t_{pd} = 1.017\sqrt{\varepsilon'_r} \quad \text{(ns/ft)}$$

or

$$t_{pd} = 85\sqrt{\varepsilon'_r} \quad \text{(ps/in.)}$$

where

$$\varepsilon'_r = \varepsilon_r\left(1 - e^{\left(\frac{-1.55B}{H}\right)}\right)$$
$$0.1 < W/H < 3.0$$
$$1 < \varepsilon_r < 15$$

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4.2.3 Single-Stripline Topology

Stripline refers to a transmission line located between two planar conductive structures, with a dielectric material completely surrounding the trace (Fig. 4.4). Consequently, stripline traces are routed internal to the board and are not exposed to the external environment.

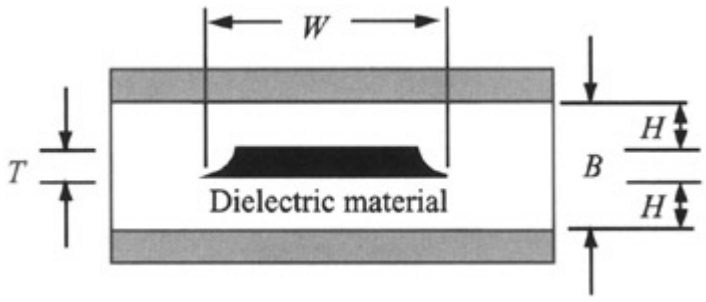

Figure 4.4: Single-stripline topology.

Stripline has several advantages over microstrip. Namely, stripline captures magnetic fields while minimizing crosstalk between routing layers. It also provides an enhanced RF current reference return path for magnetic field flux cancellation. Any radiated emissions that may occur from a routed trace will be captured by the two reference planes. Thus, reference planes significantly reduce RF energy from radiating to the outside environment.

When measuring or calculating trace impedance, the microstrip topology section should be consulted for a discussion of why we measure trace impedance of the line at the middle dimension of the trace thickness *after* etching.

The approximate characteristic impedance for single-stripline impedance is provided by Eq. (4.7) for Fig. 4.4. Intrinsic capacitance is described by Eq. (4.8). Note that Eqs. (4.7) and (4.8) are based on variables chosen for an optimal value of height, width, and trace thickness. During actual board construction, the impedance may vary by as much as ± 5% from calculated values due to manufacturing tolerances.

(4.7) $$Z_o = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) ln\left(\frac{1.9B}{(0.8W + T)}\right) = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) ln\left(\frac{1.9(2H + T)}{(0.8W + T)}\right) \quad \Omega$$

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(4.8) $$C_o = \frac{1.41\varepsilon_r}{ln\left(\frac{3.81H}{0.8W + T}\right)} \quad \text{pF/in.}$$

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where Z_o = characteristic impedance (ohms)

B = distance between both reference planes

W = width of the trace

T = thickness of the trace

H = distance between signal plane and reference plane

C_o = intrinsic capacitance of the trace (pF/unit distance)

ϵ_r = dielectric constant of the planar material

$W/(H-T) < 0.35$

$T/H < 0.25$

Note Use consistent dimensions for width, thickness, and distance spacing between planes (inches or centimeters). The value for C_o is provided in inches, which is easily converted to metric.

The propagation delay of signal stripline is described by Eq. (4.9), which has only ϵ_r as the variable.

(4.9) $$t_{pd} = 1.017\sqrt{\varepsilon_r} \quad \text{(ns/ft)}$$

or

$$t_{pd} = 85\sqrt{\varepsilon_r} \quad \text{(ps/in.)}$$

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4.2.4 Dual or Asymmetric Stripline Topology

A variation on single stripline is dual or asymmetric stripline. This topology increases coupling between a routing layer and a reference plane. When the circuit is placed approximately in the middle one-third of the interplane region, the error caused by assuming the circuit to be centered will be quite small and will fall within the tolerance range of the assembled board.

The approximate characteristic impedance for dual stripline provided in Eq. (4.10) is for Fig. 4.5. This equation is a modified version of that used for single stripline. Note that the same approximation reason for single stripline is used to compute Z_o.

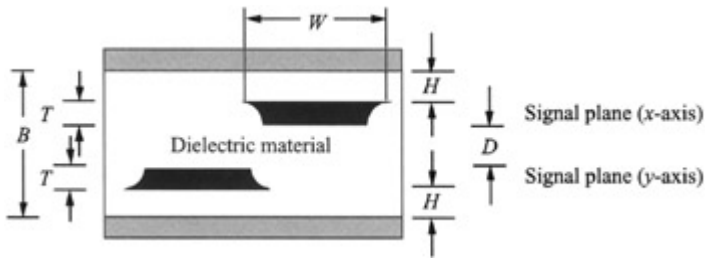

Figure 4.5: Dual or asymmetric stripline topology.

(4.10) $$Z_o = \left(\frac{80}{\sqrt{\varepsilon_r}}\right) ln\left[\frac{1.9\,(2H + T)}{(0.8W + T)}\right]\left[1 - \frac{H}{4(H + D + T)}\right] \Omega$$

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(4.11) $$C_o = \frac{2.82\varepsilon_r}{ln\left[\frac{2(H - T)}{0.268W + 0.335T}\right]}$$

Get MathML

where

Z_o	=	characteristic impedance (ohms)
H	=	dielectric thickness between signal plane and reference plane
T	=	thickness of the trace
W	=	width of the trace
D	=	distance between signal plane
C_o	=	intrinsic capacitance of the trace (pF/unit distance)
ϵ_r	=	dielectric constant of the planar material

$W/(H-T) < 0.35$

$T/H < 0.25$

Note Use consistent dimensions for width, thickness, and distance spacing between planes (inches or centimeters). The value for C_o is provided in inches, which is easily converted to metric.

Equation (4.10) can be applied to the asymmetrical (single) stripline configuration when the trace is not centered equally between two reference planes. In this situation, H is the distance from the center of the trace to the nearest reference plane. The letter D would become the distance from the center of the trace being evaluated to the other reference plane.

The propagation delay for the dual stripline configuration is the same as that for the single stripline, since both configurations are embedded in a single, homogeneous dielectric material.

(4.12)

$$t_{pd} = 1.017\sqrt{\varepsilon_r} \quad \text{(ns/ft)}$$

or

$$t_{pd} = 85\sqrt{\varepsilon_r} \quad \text{(ps/in.)}$$

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Note When using dual stripline topology, both layers must be routed orthogonal to each other. This means that one layer is provided for the *x*-axis traces, while the other layer is used for *y*-axis traces. Routing these layers at 90-degree angles to each other prevents crosstalk from developing between the two planes, especially with wide busses. High-frequency traces can cause data corruption to the alternate routing layer.

4.2.5 Differential Microstrip and Stripline Topology

Differential traces are two conductors adjacent to each other throughout the entire trace route. All differential transmission systems are theoretically immune to common-mode noise. The effects of common-mode energy on a transmission line may cause harmful operation. The impedance for differentially routed traces is not the same as a single-ended trace. For this configuration, the line-to-reference plane impedance is for *single-ended* trace routing, not *differential-mode*. In order to calculate differential-mode impedance, the single-ended value of impedance must be known ahead of time.

Differential signaling is typically used when signal return integrity through a "single-ended ground system" would be ineffective or would not allow sufficient noise margin to transmit the signal to a receiver. This is best implemented with the expectation of extremely long signal runs (amplitude loss and potential electromagnetic interference). This includes building-to-building connections (grounding instabilities) or an expected lossy situation in a shorter signaling run. This shorter signal run would, in essence, create the same sort of conditions that normally exist with an extremely long interconnect. With very high frequency and fast edge time transitions, such conditions may be present between systems.

When two traces are routed parallel to each other, magnetic field coupling occurs between the two transmission lines. The magnitude of coupling induces a current from one trace to the other. Therefore, the mutual inductance between traces will cause the differential-mode impedance to be approximately twice that of single-ended.

For Fig. 4.6, differential traces are shown. If the configuration is microstrip, an upper reference plane is not provided. For stripline, both reference planes are provided, with equal center spacing between the parallel traces and the two reference planes.

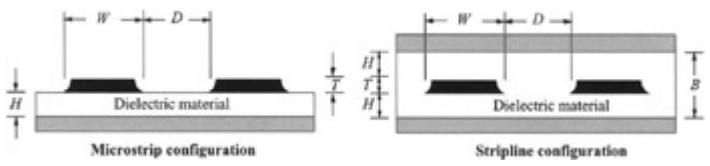

Figure 4.6: Differential trace routing topology.

When calculating differential impedance, Z_{diff}, only the trace width *W* should be altered to optimize the value of Z_{diff}. The distance spacing should not be adjusted between the two traces, identified as *D*, which should be the *minimal* spacing possible during the manufacturing process [5]. Technically, as long as the routed length of the differential pair is approximately the same, taking into consideration the velocity of propagation of the electromagnetic field within the transmission line, extreme accuracy on matched trace lengths need not occur. The speed of propagation is so great that a minor difference in routed lengths will not be observed by most components. This is true for signals that operate below 1 GHz.

(4.13)

$$Z_{diff} \approx 2 * Z_o(1 - 0.48e^{-0.96\frac{D}{H}})\ \Omega \quad \text{(microstrip)}$$

$$Z_{diff} \approx 2 * Z_o(1 - 0.347e^{-2.9\frac{D}{B}})\ \Omega \quad \text{(stripline)}$$

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where

(4.14)
$$Z_o = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}}\right) ln\left(\frac{5.98H}{0.8W + T}\right) \Omega \quad \text{(microstrip)}$$

$$Z_o = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) ln\left(\frac{1.9B}{(0.8W + T)}\right) = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) ln\left(\frac{1.9(2H + T)}{(0.8W + T)}\right) \Omega \quad \text{(stripline)}$$

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where B = plane separation
W = width of the trace
T = thickness of the trace
D = trace edge-to-edge spacing
H = distance spacing to nearest reference plane

Note Use consistent dimensions for the above (inches or centimeters). The value for C_o is provided in inches, which is easily converted to metric.

There are five reasons why differential pair traces are used:

1. *To match an external, balanced differential transmission line*. For purposes of illustration, intertrace coupling is irrelevant. Two independent 50-ohm traces will couple a signal into a 100-ohm differential pair. The application is to guarantee that the signal transmitted is purely differential. No common-mode components are to be present within the transmission line. These two traces must have equal impedance to ground; that is, they need to be symmetrical but not necessarily physically close together.

2. *To prevent ground bounce*. Differential components have a built-in reference voltage. The receiver of a differential-pair transmission line does not need to rely on an external 0-V reference. The reference could be corrupted by ground bounce or board-induced noise voltages from transmitting components. For this purpose, we need only supply the receiver with two signals, equal and opposite, with equal delays from the transmitter. There is no requirement here for particularly close coupling between traces.

3. *To reduce EMI*. Magnetic flux from one trace of the differential pair is canceled by the magnetic flux traveling in the opposite direction from the adjacent trace, resulting in a significant reduction in emissions. This cancellation is proportional to the ratio *S/D* where *S* is trace separation and *D* is the distance to the receiving antenna. For FCC Class B, at a distance of 3 meters (117 in. or 297 cm), a 1 in. (2.54 cm) separation would yield a 40-dB reduction in EMI. A 0.10 in. (0.25 cm) separation should yield 60 dB. These attenuation values are better than having a common-mode balance between the two outputs that create the differential signal. With a separation of 0.10 in., we have balanced the signal as best as possible, given imperfections in the source driver. At the 0.10 in. separation level, the reduction in emissions is at a level far below FCC limits. For EMI purposes, differential trace spacing of 0.10 in. is close enough to be adequate. We need not struggle to place the traces any closer than this distance, as far as EMI requirements are concerned.

4. *To reduce localized crosstalk*. Differential-mode traces in a PCB perform poorly at minimizing crosstalk. Signal cancellation is a function of the ratio of trace separation, *S*, to the distance of the antenna, *D*. For localized interference, there is minimal cancellation. For differential signaling, the best way to improve localized crosstalk is to move the affected traces further apart. Assuming there is a solid power and ground reference plane, crosstalk between aggressor trace and victim trace falls off as the square of distance between the two. Doubling the distance cuts crosstalk to one-fourth. Cramming two traces of a differential pair closer together increases crosstalk. The

advantage of the squared benefit from increasing the separation between aggressor and victim is more beneficial than routing differential traces close together.

5. *To improve the ability to route the PCB*. Differential traces can be routed very close together. This provides significant improvement for routability, and it saves board real estate. The desire to save board area may be a motivation for employing unusually close trace spacing. If one is committed to use of tightly packed, differential traces, two issues are to be noted:
    a. One must compute a new trace width to compensate for the fact that differential impedance goes down for closely spaced signals, and

    b. Once the signals are paired, they should not be separated. Separation alters trace impedance, unless wider trace widths are used. A second effect imposes a routing penalty on the side-by-side approach. It is hard to get traces to route around obstacles without the ability to temporarily separate. The over/under format works better for long-distance complicated routing.

Unless absolutely pressed for space, the preferred routing method is the side-by-side format (edge-coupled). These traces should be kept near each other and they may be separated from time to time, as needed, to go around obstacles such as vias while keeping both routing lengths nearly equal. Figure 4.7 illustrates two configurations of differential routing.

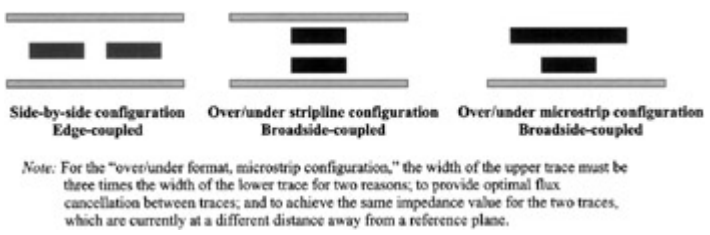
Side-by-side configuration
Edge-coupled
Over/under stripline configuration
Broadside-coupled
Over/under microstrip configuration
Broadside-coupled
Note: For the "over/under format, microstrip configuration," the width of the upper trace must be three times the width of the lower trace for two reasons; to provide optimal flux cancellation between traces; and to achieve the same impedance value for the two traces, which are currently at a different distance away from a reference plane.

Figure 4.7: Differential pair routing formats.

For the over/under format (broadside-coupled), one trace is routed above or below the other trace. There is a subtle asymmetry in this configuration. For microstrip, the physical distance to a reference plane from the top layer is greater than the physical distance to the bottom layer, or reference planes of the PCB. Any return current associated with the top layer will have to find a nearby via to provide a return path back to the top surface. The net effect is that one trace will have some extra delay built in at the endpoints. To minimize this extra delay problem, one must guarantee that ground vias are located near the point where the signals originate.

Various concerns must be noted when using edge-coupled or broadside differential pair routing, described next.

Edge-Coupled Stripline. This differential topology consists of two traces with equal widths centered between two reference planes. This configuration represents an optimal differential impedance value. The symmetry of edge-coupled stripline in all three axis of the PCB results in maximum predictability when simulation is used to analyze a design. Since traces are shielded on both sides by a reference plane, optimal noise immunity against common-mode energy is minimized. All differential transmission systems are supposed to be immune to common-mode noise.

Important concerns when using edge-coupled differential pairs include

- The physical distance between traces must be controlled during fabrication. This results in having all critical copper features (trace and distance spacing) located on only one side of a layer. The physical distance between trace after etch must be consistent. If the etching is not perfect, differential impedance can vary widely. Use of 0.5-oz copper for traces is recommended to ensure good etch results with a minimum of undercut.

- Routed traces should be centered between two reference planes, although this is not a requirement. Use of a field solver to calculate actual impedance may be required. There is no valid theoretical reason for centering the traces.

Broadside-Coupled Stripline. Broadside-coupled traces have the

advantage of relying less on a reference plane for impedance control, and they can work with no ground plane at all. For this application, broadside-coupled traces can cross a moat or partition with minimal disruption, along with other benefits and liabilities. Broadside-coupled traces are routed over/under with respect to the respective trace pair.

- Broadside-coupled transmission lines are created by having an identical routing path for the two signal lines, locating them on adjacent layers. This type of configuration opens channels for future routing, especially on logic card designs, and allows a near absence of skew between traces in the pair. Minimizing skew is a very desirable design requirement.

- Broadside-coupled transmission lines are mechanically similar to the dual stripline model for characteristic (single-ended) impedance. This impedance control makes constructive use of the interplay between overlapping circuits. The interaction between the two traces and reference planes is virtually unimportant, except to carry return currents.

- Designing a PCB with broadside-coupled transmission lines is theoretically predictable when using field solver software. These traces have poor controllability when manufactured. The dielectric thickness variation can cause transmitted signals to have nonidentical reference planes.

- The impedance is not particularly sensitive to the distance spacing to a reference plane. This sensitivity is related to the distance spacing between the surfaces of the trace pair. When the dielectric is core, differential impedance is very predictable; it is less so when it is prepreg.

- The dielectric value between the two signal pairs can become critical when routing on different layers as a trace pair. Different dielectrics may cause a variation in the differential impedance along the entire trace route.

- Layer-to-layer registration can cause a variation in differential impedance. This registration, or distance spacing between layers, can be up to 0.002 in. (0.05 mm) if the trace pair is on the same core layer and can approach 0.003 mil (0.08 mm) between core layers. This is an excellent reason to make the traces as wide as possible. If thin traces are implemented, the configuration may look more like a two-wire line. This two-wire line will have an impedance variation proportional to the log of the separation divided by the mean radius of the trace. Even in this case, the variation resulting from registration is not too serious.

If broadside-coupled pair routing must be implemented:

- Use wide line widths to cut down on the impedance variation caused by registration problems and etch-back.

- Guarantee that reference planes are on adjacent layers to the broadside-coupled trace pair. Broadside coupling need not be centered; however, the pair should be located between two reference planes. This placement will minimize common-mode energy developed within the PCB. Differential-mode current flows only within trace pairs.

- Ensure that the trace pair is located on the same core material. This helps reduce impedance variation caused by fabrication tolerances.

Both signal amplitude loss and crosstalk have a number of variables that need to be considered. This situation exists with both single-ended and differential-mode transmissions. Crosstalk is developed by either capacitive or inductive coupling. Reducing coupling would yield identical results regardless of routing topology. The same is true for signal-amplitude losses. Theoretically, DC resistance, skin effect, and dielectric losses can all be manipulated. Again, identical results would be observed.

- In certain applications, the broadside-coupled stripline is sometimes a better choice, with the drawback that routing the board may become impossible, especially on double-sided assemblies. Although it might be desirable to limit the routing of other traces in the differential pair area for crosstalk reasons, high-density application generally makes it impractical to minimize other signal routing within this area. Again, a

tradeoff assessment would be necessary to determine whether broadside-coupled traces would be applicable for a particular application.

- The effectiveness of differential signaling is dependent on the electrical balance of the pair. The design of broadside-coupled differential traces can be difficult to implement. This difficulty is due to maintaining a matched distance between the traces relative to reference planes and to each other. It is also important to maintain the etched line width on each layer. The dielectric value of all material must be consistent. If consistency cannot be guaranteed, it becomes nearly impossible to implement in a production environment.

- Edge-coupled stripline tends to have fewer variables to contend with during construction of the PCB.

- Wider trace widths are needed to keep the line impedance stable with regard to layer registration in broadside-coupled construction.

- Typically, broadside-coupled traces tend to yield lower impedance for similar dimensional constraints, compared to edge-coupled stripline. In broadside-coupled configurations, a larger dielectric distance will be required between the trace pair, and reduction of line widths may need to be implemented to achieve a desired impedance requirement. In very high-frequency applications, skin effect might have some impact on signals used with narrower trace widths.

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

IEEE Press © 2000

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4.3 PROPAGATION DELAY AND DIELECTRIC CONSTANT

Electromagnetic waves propagate at a speed that is dependent on the electrical properties of the surrounding medium. Propagation delay is typically measured in units of picoseconds/inch. Propagation delay is the inverse of velocity of propagation (the speed at which data is transmitted through conductors in a PCB). The dielectric constant, ϵ_r, varies with several material parameters. Factors that influence the relative permittivity include the electrical frequency, temperature, extent of water absorption (also forming a dissipative loss), and the electrical characterization technique. In addition, if the PCB material is a composite of two or more laminates, the value of ϵ_r may vary significantly, as the relative amount of resin and glass of the composite is varied [4].

In air or vacuum, the velocity of propagation is the speed of light. In a dielectric material, the velocity of propagation is slower, approximately 0.6 times the speed of light for common PCB laminates. Both the velocity of propagation and the effective dielectric constant equations are given by Eq. (4.15).

(4.15)
$$V_p = \frac{C}{\sqrt{\varepsilon'_r}} \qquad \text{(velocity of propagation)}$$

$$\varepsilon'_r = \left(\frac{C}{V_p}\right)^2 \qquad \text{(dielectric constant)}$$

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where V_p = velocity of propagation

C = $3*10^8$ m per second, or about 30 cm/ns (12 in./ns)

ϵ'_r = effective dielectric constant

The effective relative permittivity, ϵ'_r, is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. Effective relativity permittivity can be determined by using a Time Domain Reflectometer (TDR) or by measuring the propagation delay for a known length line and calculating the value.

Propagation delay is also a function of capacitance per unit length of line. This capacitance is a function of the dielectric constant, trace width, and thickness of the dielectric between the trace and reference plane. A trace located over a plane creates a capacitor. A capacitor is defined as two parallel plates separated by a dielectric. The difference between this capacitor and a typical capacitor is that one plate of the capacitor is only the width of the trace, whereas the other plate is a reference plane.

For FR-4, the propagation delay of a signal between a source and load for various topologies, with a dielectric constant of 4.3, based on Eqs. (4.3, 4.6, 4.9, 4.12) is presented in Table 4.1.

Table 4.1: Velocity of Propagation for Various Topologies (Dielectric Constant = 4.3)

Open table as spreadsheet

Topology	Velocity of Propagation
Microstrip	1.68 ns/ft (140 ps/in.); 0.055 ns/cm (55 ps/cm) [0.60 ft/ns (7.2 in/ps); 0.018 cm/ps]
Embedded microstrip;	2.11 ns/ft (176 ps/in.); 0.069 ns/cm (69.2 ps/cm)
Single stripline;	[0.47 ft/ns (5.6 in/ps); 0.014 cm/ps]
Dual stripline	

Embedded microstrip, single stripline, and dual stripline have the same value for propagation delay because the transmission line is completely surrounded by a dielectric. Microstrip has one-half of the transmission line in a dielectric, whereas the other one-half is in air. Therefore, the velocity of propagation of the electromagnetic wave within the microstrip transmission line is faster.

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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4.4 CAPACITIVE LOADING OF SIGNAL TRACES

When digital devices are used within a circuit, each input pin of a component contains a specific value of input capacitance. With many components, the summation of this capacitance can become substantial. This condition is identified as capacitive loading, and it affects both signal integrity and EMI. Capacitive input loading also lowers the value of the trace impedance when additional devices are added to the routed net. The unloaded propagation delay for a transmission line is defined by $t_{pd} = \sqrt{L_o C_o}$. This equation is valid when no devices are connected to the end of the net (open circuit). If a load, C_d, is placed in the transmission line (including all loads with their capacitance added together), the propagation delay, or slowing down of the signal, will increase by a factor of Eq. (4.16). This means that the signal will arrive at the load at a later time than if no loads were provided.

(4.16)
$$t'_{pd} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} \quad \text{ns/length}$$

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where t'_{pd} = modified propagation delay when capacitance is added to the circuit

t_{pd} = unmodified propagation delay, nonloaded circuit

C_d = input gate capacitance from all loads added together

C_o = characteristic capacitance of the line/unit length

For C_o, units must be per unit length, not the total line capacitance.

For example, assume a load of five CMOS components are on a signal route, each with 10-pF input capacitance (total C_d = 50 pF). In a glass epoxy board, 25-mil traces, and a characteristic board impedance Z_o = 50 Ω (t_r = 1.65 ns/ft), the characteristic capacitance of the transmission line is C_o = 35 pF. The modified propagation delay of the transmitted signal is

(4.17)
$$t'_{pd} = 1.65 \text{ ns/ft}\sqrt{1 + \frac{50}{35}} = 2.57 \text{ ns/ft}$$

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This equation gives us the total propagation delay within the transmission line due to added capacitance, *not* the added delay contributed by the capacitance. The signal arrives at its destination 0.92 ns/ft (0.19 ns/cm) later than expected (2.57 - 1.65 = 0.92 ns/ft).

The characteristic impedance of this transmission line, altered by gate loading, Z'_o, becomes

(4.18)

$$Z'_o = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}}$$

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where Z'_o = modified line impedance (ohms)

Z_o = original line impedance (ohms)

C_d = input gate capacitance—sum of all capacitive loads

C_o = characteristic capacitance of the transmission line

$$Z'_o = \frac{50}{\sqrt{1 + \frac{50}{35}}} = 32\ \Omega$$

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With 50-pF capacitance added to this transmission line, the impedance drops from 50 to 32 ohms. This lower impedance presents serious functionality concerns. These concerns include the need for greater drive current from the source driver, because the bench voltage remains unchanged with a lower trace impedance being present (Ohm's law, *V*=*IZ*).

Typical values of C_d are 5 pF for ECL inputs, 10 pF for each CMOS device, and 10–15 pF for TTL. Typical C_o values of a PCB traces are 2–2.5 pF/inch. These C_o values are subject to wide variations due to the physical geometry and the length of the trace. Sockets and vias also add to the overall distributed capacitance of the transmission line. Sockets add approximately 2-pF capacitance for each one, and vias approximately 0.3–0.8 pF each. Given that $t_{pd} = \sqrt{L_o * C_o}$ and $Z_o = \sqrt{L_o / C_o}$, total trace distributed capacitance, C_o, is calculated as

(4.19)
$$C_o = 1000 \left(\frac{t_{pd}}{Z_o} \right) \text{ pF/length}$$

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This loaded propagation delay value is one method that may be used to decide whether a trace needs be treated as a transmission line ($2 * t'_{pd} *$ trace length > t_r or t_f) where t_r is the rising edge of the signal transition and t_f the falling edge.

Distributed capacitance per length of trace, C_d, depends on the capacitive loading of all devices, including vias and sockets, if provided. To mask transmission line effects, which includes reflections, ringing, and overshoot, slower edge transition times are recommended. A heavily capacitive loaded trace slows the rise and fall times of the transmitted signal owing to an increased time constant $(\tau = ZC)$ associated with increased distributed capacitance and filtering of high-frequency components from the switching device. Notice that impedance, *Z*, is used, and not *R* (pure resistance) in the time constant equation. This is because *Z* contains *both* real resistance and inductive reactance. Inductive reactance, $(j2\pi fL)$, is much greater than *R* above several kilohertz within the transmission line, which must be taken into consideration. Heavily loaded traces seem advantageous, until the loaded trace condition is considered: lower trace impedance and greater drive current, along with a slower propagation time.

A high C_d increases the loaded propagation delay and lowers the loaded characteristic impedance. The higher loaded propagation delay increases the likelihood that transmission line effects will not be masked during rise and fall transition intervals. Lower loaded characteristic impedance often exaggerates the impedance mismatch between the driving device and the PCB trace. Thus, the apparent benefits of a heavily loaded trace are not realized unless the driving gate is designed to drive large capacitive loads [9].

Because capacitive loading alters the characteristic impedance of the trace, along with an increase in propagation delay, a high ratio between distributed and intrinsic line capacitance exaggerates the effects of loading on the characteristic impedance. Because $Z_o = \sqrt{L_o/(C_o + C_d)}$, additional loads, C_d, increases the total capacitance of the net. The loading factor, $\sqrt{1 + C_d/C_o}$, divides into Z_o, and the characteristic impedance of the transmission line decreases. Reflections within a loaded trace, causing ringing, overshoot, and switching delays, are more extreme when the loaded characteristic impedance differs substantially, especially between the driving device's output pin and the receiving device's input. The units of measurement used for capacitance and inductance are in per inch or cm units. If the capacitance used in the L_o equation is pF/in., the resulting inductance will be in pH/in.

With knowledge that adding capacitance lowering trace impedance, it becomes apparent that if a device is driving more than one line, the active impedance of each line must be determined separately. This determination must be based on the number of loads and the length of each line. Careful control of circuit impedance and reflections for trace routing and load distribution must be given serious consideration during the design and layout of the PCB.

If capacitive input loading is high, compensating a signal may not be practical. Compensation refers to modifying the transmitted signal to enhance the quality of the received signal pulse using a variety of design techniques. For example, use of a series resistor or another termination method to prevent reflections or ringing that may be present in the transmission line is one method to compensate a distorted signal. Reflections that occur with multiple transmission lines emanating from a single source must be considered at all times.

The low impedance often encountered in the PCB sometimes prevents proper Z_o (impedance) termination. If this condition exists, a series resistor in the trace is helpful. The value of the resistor needs to be as large as possible, without corrupting signal integrity. Although a 10-Ω resistor provides benefit, a 33-Ω resistor is commonly used.

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4.5 COMPONENT PLACEMENT

Clock circuits should be located near a ground stitch location (to chassis ground) on the PCB rather than along the perimeter or near the I/O section. If the transmission line goes to a daughter card, ribbon cable, or peripheral located remote from the main PCB, the transmission line must be terminated directly at the connector or boundary location. It is imperative that this be a point-to-point radial, discussed later in this chapter. Termination of traces enhances signal quality instead of the unterminated clock line being left open ended. An open-ended transmission line will energize a dipole antenna. (Trace is the driven element, and 0V-reference is the ground element.) In addition to termination, suppression of radiated RF currents coupling into other areas susceptible to RF corruption is prevented, discussed later in this chapter.

Oscillators and crystals must be installed directly on the PCB. **Do not use sockets!** Sockets add additional lead inductance (*Ldl/dt*) to the transmission line. Inductance allows a voltage potential difference to be established between the silicon die and bonding pad. This voltage potential difference develops common-mode RF energy. Sockets, like lead-length inductance, provides an additional path for radiated RF currents and harmonics to couple into areas both internal to the product and outside environment.

Only traces associated with the clock, or frequency-generating circuitry must be placed in a separate clock generation area; no other traces must be placeed "near, under, or through" this clock circuit on an adjacent signal routing layer. This route keep-out area is required only for an embedded microstrip signal layer located between a top (component) layer and first reference plane (power or ground). If a trace must be routed on a two- or four-layer board through this frequency-generating area, this trace must be routed only on the solder (bottom) side. Traces must not be routed within the vicinity of the oscillator's output pin or directly under the oscillator!

Allowance should be made for possible use of a Faraday shield (a metal enclosure that covers devices 100%) around the entire clock circuit area. Provision should be made for a ground trace circumscribing the zone (except for the point of signal trace exit, if required). This shield must be of a RF type similar to that used in UHF and microwave applications. This is best accomplished by placing ground vias around the device. In addition, there must be an additional means of grounding the metal case of oscillator modules, as the ground pin of the oscillator is usually not sufficient to source RF currents created internal to the package to ground. This ground pin was designed for use as a 0V-reference and was not designed for use as a low-impedance path to source RF currents to ground.

When placing PCB components during layout that use clocks or periodic signals, these devices must be located so that periodic signal or clock traces are routed for a best straightline path possible with minimal length and number of vias. Vias add inductance to the trace, approximately 1 to 3 nH each. Inductance in a trace may cause signal integrity concerns and potential RF emissions. The faster the edge-rate transition of a signal, the more this design rule approaches mandatory status. If a periodic signal or clock trace must traverse from one routing plane to another, this transition should occur at a component lead (pin escape) and not anywhere else, if possible, to reduce additional inductance within the transmission line from use of additional vias.

Any periodic signal or clock circuitry located within 2 in. (5 cm) of I/O components (or I/O connectors) should have edge rate transitions (t_r or t_f) slower than 10 ns, since most I/O circuits (serial, parallel, audio, and the like) are generally slow compared to other functional areas. It is recommended that traces located within 3 in. (7.6 cm) of an I/O section should have an edge rate transition between 5 and 10 ns. This general rule of locating clocks near I/O areas is not required when functional partitioning occurs (Chapter 5). This is because functional partitioning of the power and ground planes in an I/O area prevents RF currents that exist in other sections of the board from entering the I/O section. RF currents can be coupled onto I/O cables and radiated to the external environment as common-mode or differential-mode energy. Keeping RF currents created from periodic or clock signals entering I/O circuitry is the ultimate design objective.

The old directive to "keep all clock lines short" is valid. The longer the trace length, the greater the probability that RF currents will be produced and more spectral distribution of RF energy will be developed. Clock traces must be terminated to reduce ringing and creation of avoidable RF currents. This is because unterminated transmission lines generate signal reflections that can cause EMI to be generated (detailed in the next section). Clock traces might also be degraded to the point of being nonfunctional owing to transmission line effects.

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4.6 IMPEDANCE MATCHING—REFLECTIONS AND RINGING

Reflections are unwanted byproducts in digital logic designs. This section discusses why reflections are unwanted. Ringing within a transmission line contains both overshoot and ringing before stabilizing to a quiescent level and is a manifestation of the same effect. *Overshoot* is the effect of an excessive voltage level above the power rail or below the ground reference. Excessive voltage levels below ground reference are still identified as overshoot. *Undershoot* is a condition that occurs when the voltage level does not reach the desired amplitude for both maximum and minimum transition levels. Components must have a sufficient tolerance rating to voltage margin requirements. Overshoot can be controlled by terminations and proper PCB and IC package design. Overshoot, if severe enough, can overstress devices and cause damage or failure. Overshoot and undershoot are illustrated in Fig. 4.8.

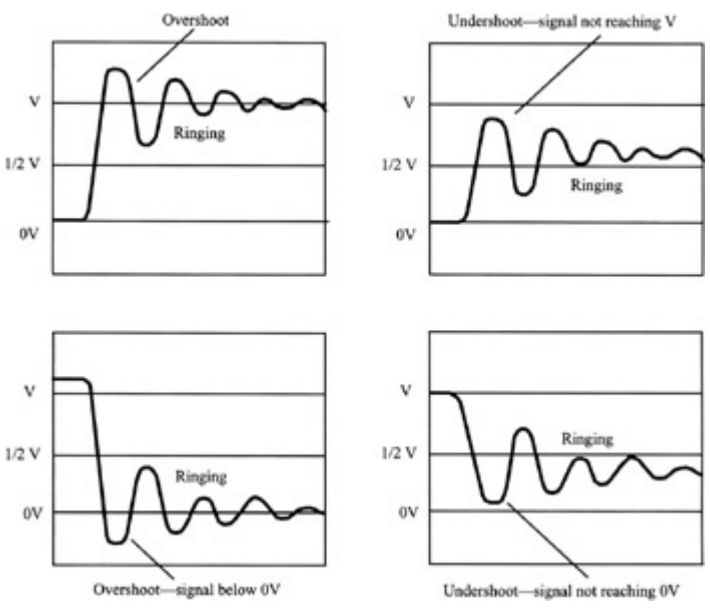

Figure 4.8: Overshoot, undershoot, and ringing

classification.

As signal edges become faster, consideration must be given to propagation and reflection delays of the routed trace. If the propagation time and reflection within the trace are longer than the edge transition period, an *electrically long trace* will exist. This electrically long trace can cause signal integrity problems, depending on the type and nature of the signal. These problems include crosstalk, ringing, and reflections. EMI concerns are usually secondary to signal quality when referenced to electrically long lines. Although long traces can exhibit resonances, suppression and containment measures implemented within the product may mask EMI energy present. Therefore, components may cease to function properly if impedance mismatches exist in the system between source and load.

Reflections are frequently both a signal integrity and an EMI issue, when the edge time of the signal constitutes a significant percentage of the propagation time between the device load intervals. Solutions to reflection problems may require extending the edge time (slowing the edge rate) or decreasing the distance between load device intervals.

Reflections from signals on a trace are one source of RF noise within a network. Reflections are observed when impedance discontinuities exist in the transmission line. These discontinuities consist of

- Changes in trace width.
- Improperly matched termination networks.
- Lack of terminations.
- T-stubs or bifurcated traces.[2]
- Vias between routing layers.
- Varying loads and logic families.
- Large power plane discontinuities.
- Connector transitions.
- Changes in impedance of the trace.

[2]A bifurcated trace is a single trace that is broken up into two traces routed to different locations.

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4.7 CALCULATING TRACE LENGTHS (ELECTRICALLY LONG TRACES)

When creating transmission lines, designers need to be able to quickly determine whether a trace routed on a PCB can be considered electrically long *during the component placement process*. If a transmission line is electrically long, signal integrity and EMI concerns develop. An electrically long trace is defined as a transmission line that is sufficiently long physically that a propagated electromagnetic wave that is sent from a source to load with its return back to the source occurs after the next edge transition. In other words, a second edge transition is injected into the transmission line prior to the return of the previous edge-triggered event.

A simple calculation is available that determines whether the *approximate* length of a routed trace is electrically long, under typical conditions. When determining whether a trace is electrically long, we must think in the *time domain*. The equations in this section are best used when doing *preliminary* component placement. For extremely fast edge rates, detailed calculations are required based on the actual dielectric constant value of the core and prepreg material. The dielectric constant determines the velocity of propagation of a transmitted wave.

The typical velocity of propagation of a signal within a transmission line, using FR-4, is 60% the speed of light. The maximum permissible unterminated line length per Eq. (4.20) must be calculated to determine if termination is required in the transmission line. This equation is valid when the two-way propagation delay (source-load-source) equals or exceeds the signal rise-time transition, or edge rate. Use the faster value of the two edge transitions, HI-LOW or LOW-HI.

(4.20)

$$l_{\max} = \frac{t_r}{2\,t'_{pd}}$$

Get MathML

where t_r = edge rate (ns)

t'_{pd} = propagation delay (ns)

$l_{\max}$ = maximum routed trace length (cm)

Figure 4.9 illustrates Eq. (4.20) for quick reference with a dielectric constant of 4.6 used within the equation.

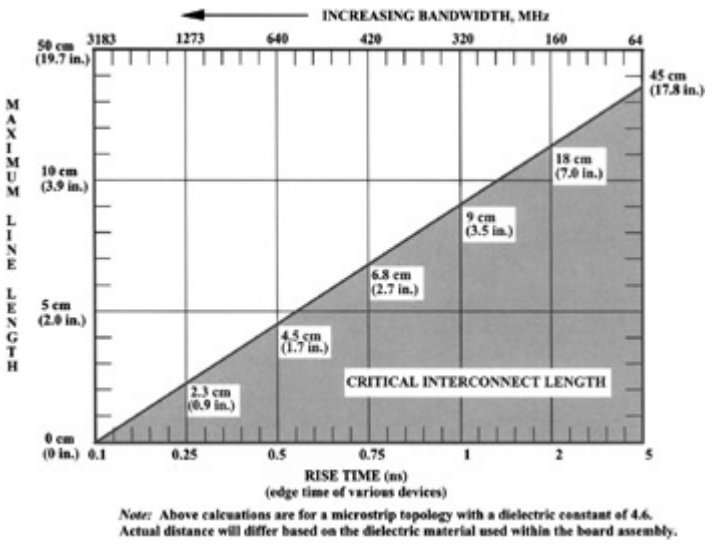

Figure 4.9: Maximum unterminated line length vs. signal edge rate (FR-4 material).

The equation is very *liberal*, since it considers only a single, two-way propagation time interval. A more conservative approach would be to consider more "round trips." In other words, the 2 in the denominator may be replaced by a 4, 6, or even 8.

To simplify Eq. (4.20), the real value of the propagation delay within the transmission must be determined using the *actual* dielectric constant value based at the frequency of interest. Both propagation delay and edge transition rate must be taken into account. Equations (4.21) and (4.22) are presented for determining the maximum routed electrical line length before termination becomes mandatory. This length is for round-trip distance. The one-way length from source to load is one-half the value of l_{max} calculated.

The factor (k) used in the calculation is for a dielectric constant value of 4.6.

(4.21) $l_{max} = k * t_r = 9 * t_r$ (for microstrip topology—in cm)
$l_{max} = k * t_r = 3.5 * t_r$ (for microstrip topology—in inches)

➡ Get MathML

(4.22) $l_{max} = k * t_r = 7 * t_r$ (for stripline topology—in cm)
$l_{max} = k * t_r = 2.75 * t_r$ (for stripline topology— in inches)

➡ Get MathML

For example, if the minimum edge rate signal transition is 2 ns, the maximum round-trip, unterminated trace length possible before termination is required, when routed microstrip is

$$l_{max} = 9 * t_r = 18 \text{ cm } (7 \text{ inches})$$

➡ Get MathML

When routed stripline, the maximum unterminated trace length of this same 2 ns signal edge becomes

$$l_{max} = 7 * t_r = 14 \text{ cm } (5.5 \text{ inches})$$

➡ Get MathML

These equations are useful when evaluating propagational time intervals between load intervals on a line with multiple devices. Figure 4.9 illustrates the relationship between rise-time transition and maximum line length distance before termination is required.

To calculate the constant "k," (9 or 7) found within Eqs. (4.21) and (4.22), use the following example:

$$k = x\left(\frac{a}{t_{pd}}\right)$$

➡ Get MathML

where k = constant factor for transmission line length determination

a = 30.5 for cm, 12 for inches

x = 0.5 (converts transmission line to one way path)

t_{pd} = $1.017\sqrt{0.475\,\varepsilon_r + 0.67}$ (for microstrip), $1.107\sqrt{\varepsilon_r}$ (for stripline)

Example: with $\epsilon_r = 4.6$, k = 8.87 for microstrip (in cm) or 3.49 (in inches)

k = 6.99 for stripline (in cm) or 2.75 (in inches)

If a trace or routed interval is longer than l_{max}, termination should be implemented, for signal reflections (ringing) may occur within this electrically long trace. Even with optimal termination, a finite amount of RF currents can still be in the trace. For example, use of a series termination resistor will achieve the following:

- Minimize RF currents within the trace.
- Absorb reflections (ringing).
- Match trace impedance.
- Minimize overshoot and undershoot.
- Reduce RF energy generated by slowing the edge rate of the clock signal.

When locating components during layout that use clock or periodic waveform signals, these components must be positioned to allow for the best straight-line path possible, with minimal trace length and number of vias in the route. Each via will add inductance to the trace, approximately 1–3 nH each. Inductance in a trace may also cause signal integrity concerns, impedance mismatches, and potential RF emissions. Inductance in a trace allows this wire to act as an antenna. The faster the edge rate of the signal transition, the more important this design rule becomes. If a periodic signal or clock trace must traverse from one routing plane to another, this transition should occur at a component lead (pin escape or breakout) and not anywhere else. If possible, additional inductance presented to the trace can be reduced from using fewer vias.

Equation (4.23) is used to determine whether a trace, or loading interval, is electrically long and requires termination.

(4.23) $$l_d < l_{\max}$$

Get MathML

where l_{max} is the calculated maximum trace length and l_d is the length of the trace route as measured in the actual board layout. Keep in mind that l_d is the round-trip length of the transmission line.

Ideally, trace impedance should be kept at ± 10% from nominal. In some cases, ± 20–30% may be acceptable only after careful consideration has been given to signal integrity and performance. The width of the trace, its height above a reference plane, dielectric constant of the board material, plus other microstrip and stripline constants determine the impedance of the transmission line. It is always best to maintain constant impedance control at all times in any dynamic signal condition.

An example used to determine whether it is necessary to terminate a signal trace using characteristic impedance, propagation delay, and capacitive loading is now presented [9].

Microstrip Example

A 5 ns edge rate device is provided on a 5 in. surface microstrip trace. Six loads (components) are distributed throughout the route. Each device has an input capacitance of 6 pF. Is termination required for this route?

Geometry

Trace width, *W*=0.010 in.

Height above a plane, *H*=0.012 in.

Trace thickness, *T*=0.002 in.

Dielectric constant, $\epsilon_r = 4.6$

A. *Calculate characteristic impedance and propagation delay [Eqs. (4.1) and (4.3)]*.

$$Z_o = \left(\frac{79}{\sqrt{\varepsilon_r + 1.41}}\right) ln\left(\frac{5.98\,H}{0.8\,W + T}\right)$$

$$Z_o = \left(\frac{60}{\sqrt{4.6}}\right) ln\left(\frac{1.9 \times 20}{0.8(6) + 1.4}\right) = 50.7\ \Omega$$

$$t_{pd} = 1.017 * \sqrt{0.475\,\varepsilon_r + 0.67} = 1.72 \text{ ns/ft } (0.143 \text{ ns/in.})$$

➡ Get MathML

B. *Analyze capacitive loading*.

Calculate C_d, distributed capacitance (total normalized input capacitance divided by length).

$$C_d = (6 * C_d)/\text{trace length} = (6 * 6 \text{ pF}) / 5 \text{ in.} = 7.2 \text{ pF/in.}$$

➡ Get MathML

Calculate intrinsic capacitance of the trace—Eq. (4.19).

$$C_o = 1000\,(t_{pd}/Z_o) = 1000\,(1.72/63.5) \text{ ns/ft} = 27.0 \text{ pF/ft} = 2.26 \text{ pF /in.}$$

➡ Get MathML

Calculate one-way propagation delay time from the source driver—Eq. (4.16).

$$t'_{pd} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}}$$

$$t'_{pd} = 0.143\ \sqrt{1 + 7.2/2.26} = 0.29 \text{ ns/in. } (3.5 \text{ ns/ft})$$

➡ Get MathML

C. *Perform transmission line analysis*.

Ringing and reflections are masked during edge transitions if

$$(2 * t'_{pd}) * \text{trace length} \leq t_r \text{ or } t_f$$

➡ Get MathML

For this situation,

$$(2 * t'_{pd}) * \text{trace length} = (2 * 0.29 \text{ ns/in.}) * 5 \text{ in.} = 2.9 \text{ ns}$$

➡ Get MathML

Given that the edge rate of the component is $t_r = t_f = 5$ ns and propagation delay is 2.9 ns, termination is not required. Sometimes the guideline of (3 * t'_{pd} * trace length) is used as a margin of safety. For this case, propagation delay would be 4.35 ns; hence, termination would still not be needed.

Assume now that the trace is routed stripline. Is termination required?

From above:

$t_{pd} = 1.017 \times \sqrt{\varepsilon_r} = 2.18$ ns/ft = 0.18 ns/in.
$C_o = (t_{pd}/Z_o = 2.18/63.5 = 34.3$ pF/ft (2.86 pF/in.)
$C_o = 1000(t_{pd}/Z_o) = 1000(2.18/63.5) = 34.3$ pF/ft (2.86 pF/in.)
C_d is the same as above (7.2 pF/in.)
$t'_{pd} = t_{pd}\sqrt{1 + C_d/C_o} = 4.05$ ns/ft (0.34 ns/in.)
$2 \times t'_{pd} \times$ trace length $= 2 \times 0.34$ ns/in. $\times 5 = 3.4$ ns

➡ Get MathML

Again, this trace would not require termination since 3.4 ns $\leqslant$ 5 ns. The propagation delay for stripline is 1.60 ns longer because t_{pd} (unloaded) is substantially greater than microstrip (0.65 ns margin). This factor helps prevent transmission line effects from being masked during edge rate changes.

Stripline Example

A 2-ns edge rate device on a 10 in. stripline trace is used. Five logic devices are distributed throughout the route. Each device has an input capacitance of 12 pF. Is termination required for this route?

Geometry

Trace width, W = 0.006 in.

Distance from a plane, H = 0.020 in.

Trace thickness, T = 0.0014 in.

Dielectric constant, ϵr = 4.6

A. *Calculate characteristic impedance and propagation delay . [Eqs. (4.7) and (4.9).]*

$$Z_o = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) ln \left(\frac{1.9\,B}{(0.8W + T)}\right)$$

$$Z_o = \left(\frac{60}{\sqrt{4.6}}\right) ln \left(\frac{1.9 \times 20}{0.8(6) + 1.4}\right) = 50.7\ \Omega$$

$$t_{pd} = 1.017\sqrt{\varepsilon_r} = 2.18 \text{ ns/ft} \quad (0.182 \text{ ns/in.})$$

➡ Get MathML

B. *Analyze capacitive loading*.

Calculate C_d, distributed capacitance (total input capacitance divided by length).

$$C_d = (6 * C_d) \text{ / trace length} = (6 * 12 \text{ pF}) / 10 \text{ in.} = 7.2 \text{ pF/in.}$$

➡ Get MathML

Calculate the intrinsic capacitance of the trace.

$$C_o = 1000\ (t_{pd} / Z_o) = 1000\ (0.182/50.7) = 3.58 \text{ pF/in. } (43.0 \text{ pF/ft})$$

➡ Get MathML

Calculate one-way propagation delay time from the source driver.

$$t'pd = tpd\sqrt{1 + 7.2/3.58} = 0.32 \text{ ns/in. } (3.79 \text{ ns/ft})$$

➡ Get MathML

C. *Perform transmission line analysis*.

The important condition of interest is (2 * t'_{pd}) * trace length $\leqslant$ t_r or t_f

$$(2 * t'_{pd}) * \text{trace length} = 2 * 0.32 \text{ ns/in.}) * 10 \text{ in.} = 6.4 \text{ ns}$$

➡ Get MathML

Since the edge rate of the component t_r = t_f = 2 ns, and propagation delay (6.4 $\geqslant$ 2), termination is required to absorb transmission line effects.

Assume the trace is routed microstrip. Is termination required?

From above:

$t_{pd} = 1.017 \times \sqrt{0.475\,\varepsilon_r + 0.67} = 0.14$ ns/in. (1.72 ns/ft)
$C_o = 1000\,(t_{pd}/Z_o) = 1000(0.14/50.7) = 2.76$ pF/in. (33 pF/ft)
C_d is the same as above (7.2 pF/in.)
$t'_{pd} = t_{pd}\sqrt{1 + C_d/C_o} = 0.26$ ns/in. (3.19 ns/ft)
$2 \times t'_{pd} \times$ trace length $= 2 \times 0.26$ ns/ft $\times$ 10 in. $= 5.20$ ns

➡ Get MathML

Again, this trace would require termination since 5.20 ns $\geqslant$ 2 ns.

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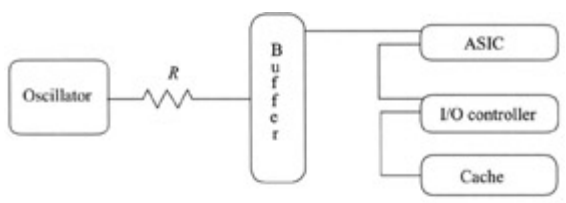
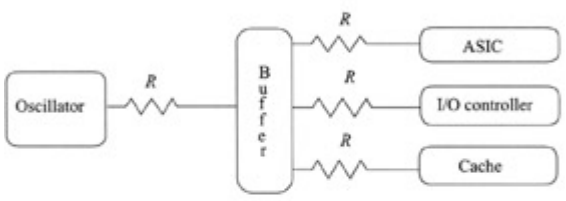
4.8 TRACE ROUTING

4.8.1 Single-Ended Transmission Lines

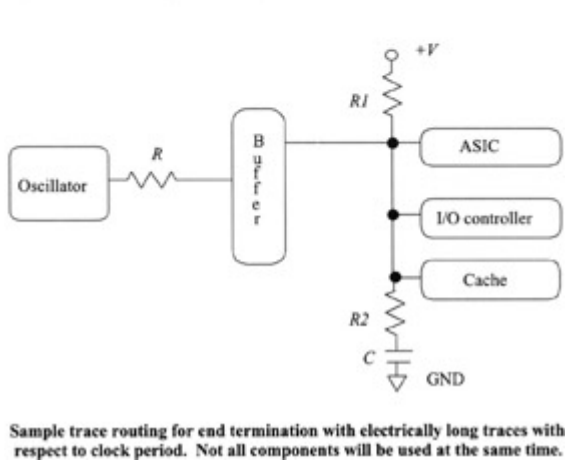
Engineers and designers sometimes daisy-chain traces for ease of routing. Unless the distance is small between loads, with respect to propagation length and signal edge transitions, signal integrity concerns may develop. These concerns include ringing and reflection. Daisy-chaining may also impact signal quality and EMI spectral energy distribution to the point of nonfunctionality or noncompliance. Therefore, radial connections for fast edge transition signals are preferred over daisy-chaining for nets with a single, common drive source. Radial connection refers to a single point-to-point connection from a driver capable of sourcing multiple loads simultaneously. Each component must have its respective trace terminated in its characteristic impedance as shown in Fig. 4.10, using a termination method appropriate for circuit operation.



Poor trace routing for clock signals (Note daisy-chaining of clock signal.)



Optimal trace routing for clock signals with series termination resistors



Sample trace routing for end termination with electrically long traces with respect to clock period. Not all components will be used at the same time.

Figure 4.10: Termination of clock traces.

If an electrically long signal trace route must be implemented, this trace *must be properly terminated*. Long transmission lines generally require use of high-current driving components. One should calculate the terminating resistor value at the Thevenin equivalent or characteristic impedance of the trace. Use of "T-stubs" or bifurcated lines is generally not allowed. A bifurcated trace is a single trace that is broken up into two traces routed to different locations. Each T-stub trace will have a characteristic impedance of $2Z_o$. This impedance discontinuity may cause signal integrity concerns, especially if the length of the stubs differs.

If a T-stub must be used, the maximum permissible stub length cannot

exceed $T = L_d^{t_r/10}$, where L_d is the routed length of the trace and t_r is the signal transition time or edge rate. The length of each "T" from the center leg must be identical. With T-stubs, both capacitance and load characteristics of components at the end of each stub must be exactly equal.

If a T-stub is required because of problems with layout or routing, stub lengths must be as short as possible. Components must be relocated to remove stubs created by an auto-placer. For applications where only a T-stub is possible, it becomes mandatory that both legs of the "T" be *exactly identical in length! Note:* This is rarely a satisfactory approach. Use the measurement feature of the CAD system to measure actual routed length. If necessary, serpentine route the shorter trace of the two stubs until this trace equals its counter trace length exactly. This is owing to the fact that a reflected wave always occurs on a signal trace. Two traces mean there will be two reflected waves. Both waves will meet at the "T" connection on their return, usually with an amplitude or phase difference that will cause serious problems to develop at the junction, all the way back to the source.

A potential or fatal drawback of using T-stubs lies in future changes to the artwork. If a different PCB designer makes a change to the layout or routing to implement rework or a redesign, knowledge of this T-stub implementation may not be known. Accidental changes to the layout may occur, posing potential EMI or signal integrity problems.

4.8.2 Differential Pair Signaling

Differential pair signaling is designed to transmit logic signals between two systems (box-to-box, box-to-peripheral) that are referenced to *different ground offsets* by an amount too large for single-ended signals to function correctly. Consequently, the driver and receiver are designed to float with respect to ground. The receiver will always have a very large input signal gain. Thus, low-voltage-level transmissions are possible, even when severe attenuation is present in the transmission line.

An advantage of differential signaling is reduced EMI. This reduction exists because the magnetic field produced by one signal trace is canceled out by its corresponding trace. This occurs because the differential signals are equal and opposite (definition of differential mode). Differential-mode transmission first became popular with use of ECL devices. Another benefit of differential signaling is immunity from common-mode energy coupling into the wire pair by external sources. This is owing to both signal traces being exposed to the same energy source, resulting in removal of the unwanted energy from the trace pair.

The objective of differential signaling is to deliver two clean signals from the driver to the receiver, regardless of how they travel, theoretically. This means that the trace pair can be side-by-side, spread apart, or routed on different layers. As long as the two signals arrive in good condition within the timing tolerance of the circuit, operation is assured. Notice that maintaining the traces to a certain impedance value is not mandatory, as long as the signal amplitude and phasing are proper for system operation at the receiver. This is shown in Fig. 4.11.

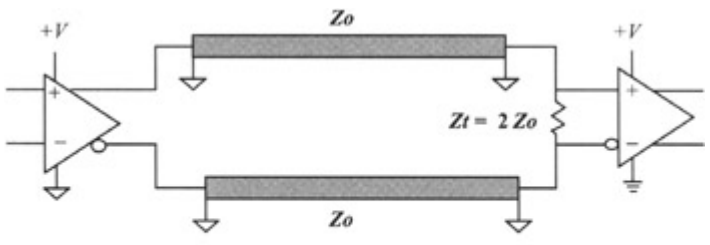

+V
Zo
+V
Zt = 2 Zo
Zo
Route each trace as a standalone transmission line.
Match length of each trace within the limits set by the manufacturer.
Center of the termination resistor goes to a virtual ground not shown.

Figure 4.11: Routing differential signal traces.

Certain logic families place a requirement on maintaining specific differential impedance between signal pairs. The ground and signal reference levels of the two devices in the figure are different, illustrating why differential signal transmission is required for certain applications.

Routing requirements for differential signaling need not be tightly controlled for most applications. Many design rules mandate that the routed trace be

within 0.100 in. (2.5 mm) of each other. This requirement makes it very difficult to route when changing layers or traveling around vias and other discontinuities. Length matching needs to be accurate enough only to prevent timing problems. A signal routed microstrip travels at a velocity of 1.68 ns/ft (0.140 ns/in. (0.36 ns/cm). For stripline, velocity of propagation is 2.11 ns/ft (0.176 ns/in. or 0.45 ns/cm). With knowledge of the velocity of propagation within the PCB for all but the fastest differential signaling protocols, length matching need not be more precise than 0.500 in. (1.27 cm). This relaxation in maintaining exact trace length for differential pair transmission lines allows for ease of autorouting and placement of vias. With use of LVDS logic, operating at 250 ps, length matching would need to be within an accuracy of *1.5 in. (3.8 cm)* or less [3].

Successful routing of differential signaling requires that the differential impedance between the two traces be properly terminated. These two transmission lines must also be equal in length, to within the timing tolerances of the logic family being used. No appreciable electrical benefit to routing two traces side by side exists, except for certain applications related to signal integrity. However, if traces are not routed parallel to each other, serious EMI concerns develop.

Four concerns are present when routing differential signals between different layers:

1. *Impedance control*. When jumping layers, an impedance discontinuity is injected into the transmission line. This impedance discontinuity may cause reflections to be developed if the termination is not properly chosen. A different number of vias may exist between the two signal pairs, thus skewing signal integrity.

2. *Return currents and layer jumping*. Flux cancellation for the return current may not be optimal, especially for certain configurations. Assume a double-sided PCB with no power and ground plane. Separating the differential pair will result in *significant* development and propagation of RF energy. For multilayer assemblies, the return current may not have an optimal, low-impedance return path, thus allowing a RF loop to exist. For long routed traces, this loop could be significant. Common-mode RF energy is now developed.

3. *Velocity of propagation*. Traces routed microstrip will propagate between source and load faster than stripline. With faster propagation of the electromagnetic wave, the microstrip signal may appear at the receiver long before the stripline signal, outside the timing margin of the circuitry, even when using matched trace lengths.

4. *Development of common-mode energy*. If a receiver is not the immediate load, but through interconnects to a cable or connector assembly (e.g., backplane configuration), a capacitive load will be presented to the trace. This capacitive load can cause the differential-mode signal to be converted to common mode at the boundary location, exacerbating EMI.

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

IEEE Press © 2000

Recommend this title? yes no

4.9 ROUTING LAYERS

PCB designers need to determine which signal layers to use for routing clocks and periodic signals. Clocks and periodic signals must be routed on either one layer or on an adjacent layer separated by a same potential reference plane. An example of routing a trace between layers is shown in Fig. 4.12. Three issues must be remembered when selecting routing layers: deciding which layers to use for trace routing, jumping between designated layers, and maintaining constant transmission line impedance.

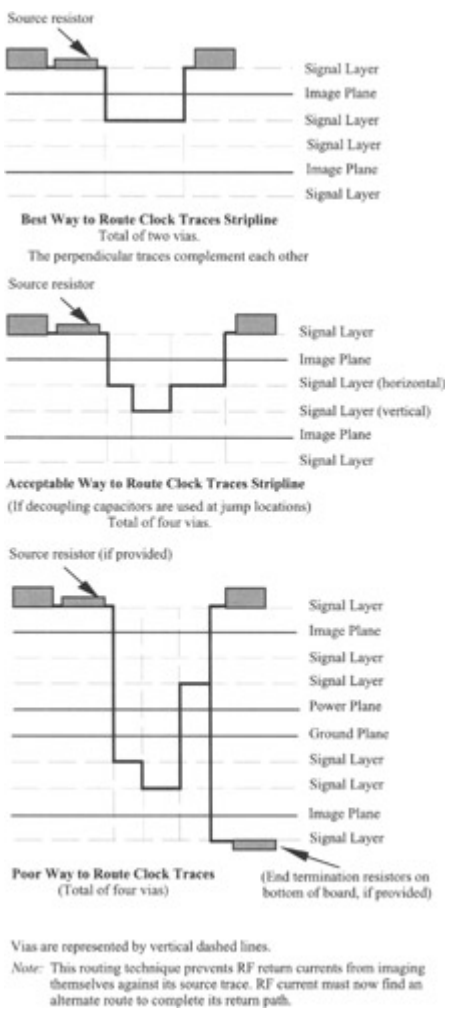
Source resistor
Signal Layer
Image Plane
Signal Layer
Signal Layer
Image Plane
Signal Layer
Best Way to Route Clock Traces Stripline
Total of two vias.
The perpendicular traces complement each other
Source resistor
Signal Layer
Image Plane
Signal Layer (horizontal)
Signal Layer (vertical)
Image Plane
Signal Layer
Acceptable Way to Route Clock Traces Stripline
(If decoupling capacitors are used at jump locations)
Total of four vias.
Source resistor (if provided)
Signal Layer
Image Plane
Signal Layer
Signal Layer
Power Plane
Ground Plane
Signal Layer
Signal Layer
Image Plane
Signal Layer
Poor Way to Route Clock Traces
(Total of four vias)
(End termination resistors on bottom of board, if provided)
Vias are represented by vertical dashed lines.
Note: This routing technique prevents RF return currents from imaging themselves against its source trace. RF current must now find an alternate route to complete its return path.

Figure 4.12: Example of routing layers for clock signals.

4.9.1 Which Layers to Route Traces On

Figure 4.12 is a representative sample of how to route sensitive, or high-threat, traces.

1. Use a solid image or reference plane/trace adjacent to the signal route. Minimize trace length routing while maintaining a controlled impedance value of the transmission line. If series termination is used, connect the resistor directly to the pin of the driver without use of a via between resistor and component. After the resistor, *now* place a via to the internal stripline layers.

2. Do not route clock or other sensitive traces microstrip on a multilayer board. The outer layers of a PCB is generally reserved for large signal buses and I/O circuitry. The functional signal quality of these traces could be corrupted by placing traces containing high levels of RF energy using microstrip routing. When routing traces on outer levels, a change in the distributed capacitance of the trace, as the trace relates to a reference plane may occur, thus affecting performance

and possible signal degradation.

3. Maintain constant trace impedance and minimize or eliminate use of vias, so that the trace will not radiate any more than a coax. When we reference a routing plane containing an electric field to an image plane, magnetic flux within the transmission line is canceled differentially owing to its image within the return plane, thus minimizing development of emissions. A low-impedance RF return path adjacent to the routed trace performs the same function as the braid or shield of a coax.

Three phenomena by which planes and hence, PCBs, create EMI are enumerated next. Proper understanding of these concepts will allow the designer to incorporate suppression techniques on *any* PCB in an optimal manner.

1. Discontinuities in the image plane due to the use of vias and jumping clock traces between layers. The RF return current will be diverted from having a direct-line RF return path, creating a loop antenna.

2. Peak surge currents injected into the power and ground network (image planes) due to components switching output signals. These surge current spikes propagate throughout the PCB, which is what we do not want.

3. Flux loss into the annular keep-out region of vias if *3-W* routing is not provided for the trace route. Physical separation of a trace from a via must also conform to *3-W* spacing. The *3-W rule* is discussed in the next section. This requirement prevents RF energy (magnetic flux) that is present within a transmission line (trace) from coupling into the via. This via may contain a static signal, such as reset, and may re-propagate RF energy throughout the PCB into areas susceptible to RF disruption.

The advantages and disadvantages of routing clock traces microstrip and stripline are shown in both Figs. 4.13 and 4.14.

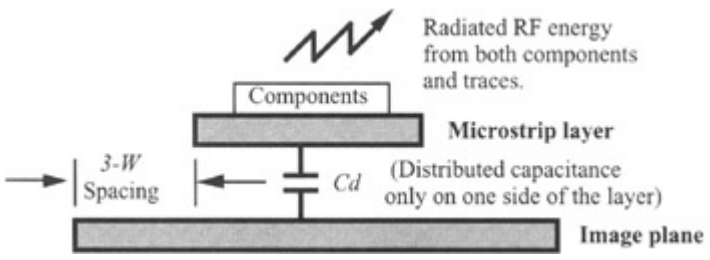

Figure 4.13: Routing clock traces microstrip.

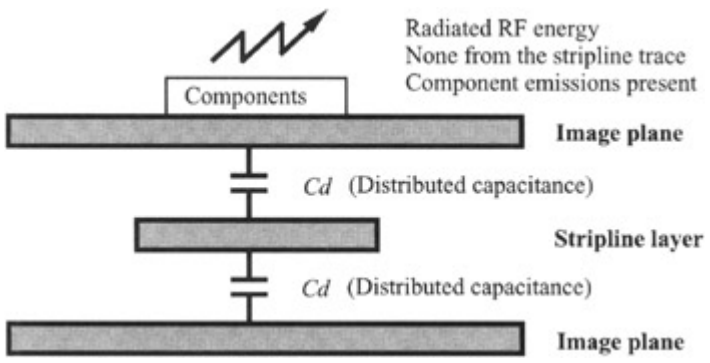

Figure 4.14: Routing clock traces stripline.

- *Microstrip*. Microstrip permits faster propagation of signals because there is less distributed capacitance between the trace and its closest reference plane. Capacitance rounds off or slows clock edges. The other side of the transmission line is air. Hence, no capacitance is present for the top half of the trace. In addition to less distributed capacitance, the propagational speed of the electromagnetic wave is accelerated. This faster speed results because the transmission line is sending an electromagnetic wave through a dielectric that is present on only one side of the trace. With less dielectric to travel through, the signal will propagate faster.

  The negative aspect of routing traces microstrip is that any RF energy generated within a transmission line can radiate to the environment. Although the trace may be electrically short and properly terminated, the RF energy developed might not be from the trace but from the components (digital logic) that drive the transmission line. Components

consist of a silicon die and lead-bond wires encapsulated within a package. Common-mode energy developed internal to the component will most likely be the cause of EMI, not the trace itself. The same radiated effect will be observed on periodic signal traces that are routed stripline, if proper layout techniques are not implemented. The majority of EMI problems observed in high-speed products is from component radiation, not trace radiation.

- Stripline is optimal for suppression of RF currents developed within the signal trace. This suppression of radiated energy is the result of having image planes on both sides of the trace. Because magnetic flux is present within the transmission line, these fields become captured by the adjacent planes. Because of skin effect, the energy absorbed will be observed only on the internal skin of the metallic conductor. RF energy cannot travel through solid planar structures.

  Routing signals stripline also cause a decrease in signal propagation between source and load. Slowing of the electromagnetic field is due to additional distributed capacitance present on *both* sides of the transmission line. Unlike microstrip, with distributed capacitance on only one side of the trace, the additional capacitance on both sides may be enough to affect the propagation speed of the signal. Signal transition edges in the nanosecond and sub-nanosecond range may be skewed by this capacitive effect. In addition, stripline signals are surrounded 100% by a dielectric, which is another factor in slowing down the propagational speed.

Note, however, that component (circuit device) radiation is not eliminated. When using stripline, components are still outside the envelope of protection provided by both planes. In most applications, components dominate as a source of RF energy. This is certainly true of through-hole devices. This component-specific radiation can be significant, requiring containment measures to be implemented.

4.9.2 Layer Jumping—Use of Vias

When routing clock or high-threat signals, it is common practice to via the trace to a routing plane (e.g., *x*- or horizontal axis) and then via this same trace to another plane (e.g., *y*- or vertical axis) from source to load. It is generally assumed that if each and every trace is routed adjacent to an RF return path, there will be tight coupling of common-mode RF currents along the entire trace route. In reality, this assumption is partially incorrect.

As a signal trace jumps from one layer to another, RF return current tries to mirror image the trace route. When a trace is routed internal to a PCB between two planar structures, commonly identified as the power and ground planes, or two planes with the same potential, return current is shared between these two planes. Return current can jump between different potential planes only at a location where there are decoupling capacitors. If both planes are at the same potential (0V-reference), the RF return current jump will occur at a location where a via connects both 0V-references planes together, using the component's ground pin assigned to that via.

When a jump is made from a horizontal to a vertical layer, the RF return current *cannot* fully make this jump. This is because a discontinuity was placed in the trace route by a layer jump. The return current must now find an alternate, low-inductance (impedance) path to complete its route. This alternate path may not exist in a position that is immediately adjacent to the location of the layer jump, or via. Therefore, RF currents on the signal trace can couple to other circuits and pose problems as both crosstalk and EMI. Use of vias in a trace route will always create a concern in any high-speed design.

To minimize development of EMI and crosstalk owing to layer jumping, the following design techniques have been found effective:

1. Route all clock and high-threat signal traces on only one routing layer as the initial approach concept. This means that both *x*- and *y*-axis routes are in the same plane. (*Note:* The PCB designer will likely reject this technique as unacceptable, because it makes autorouting of the board nearly impossible.)

2. Verify that a solid RF return path is adjacent to the routing layer, with no discontinuities in the route created by use of vias or jumping the trace to another routing plane.

If a via must be used for routing a sensitive trace, high-threat or clock signal between the horizontal and vertical routing layer, ground vias must be incorporated at "each and every" location where the signal axis jumps are executed. A ground via is always at 0V-potential. A ground via is a via placed directly adjacent to each signal route jump from the horizontal to a vertical routing layer. Ground vias can be used only when there is more than one 0V-reference plane internal to the PCB. This via is connected to all ground planes (0V-reference) that serve as the RF return path for signal return currents. This via ties all 0V-reference planes together adjacent, and parallel to, the signal trace jump location. When two ground vias are used per signal trace, a continuous RF path will be present for the return current throughout its entire trace route.[3]

What happens when only one 0V-reference (ground) plane is provided and the alternate plane is at voltage potential, commonly found with four-layer stackups? To maintain a constant return path for RF currents, the 0V (ground) plane should be allowed to act as the primary return path. The majority of the signal trace must be routed against this 0V-plane. When the trace routes against the power plane, after jumping layers, use of a *ground trace* is required only on the layer adjacent to the power plane layer. This ground trace must connect to the ground plane, by vias, at both ends. This trace must also be parallel to the signal trace at a distance spacing that is as close as manufacturable. Using this configuration, we now maintain a constant RF return path throughout the entire route (Fig. 4.15).

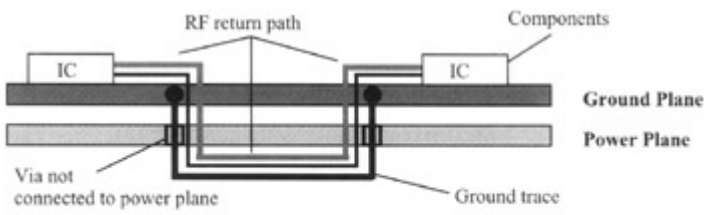
RF return path
Components
IC
IC
Ground Plane
Power Plane
Via not
connected to power plane
Ground trace
Ground trace routed adjacent to power plane connected to the main ground plane by via to guarantee undisturbed RF return path.
Four-layer PCB with trace routed on top and bottom layer

Figure 4.15: Routing a ground trace to assure a complete RF return path exists.

How can we minimize the use of ground vias when layer jumping is mandatory? In a properly designed PCB, the first traces to be routed are clock or high-threat signals, which must be "manually routed!" The PCB designer is permitted much freedom in routing the first few traces. The designer is then able to route the rest of the board using direct-line routing (shortest Manhattan length). These first few routed traces must make a layer jump adjacent to the *ground pin via* of a component. This layer jump will co-share this component's ground pin. This joint ground pin will provide both 0V-references to the component, while allowing RF return current to make the layer jump, as detailed in Fig. 4.16.

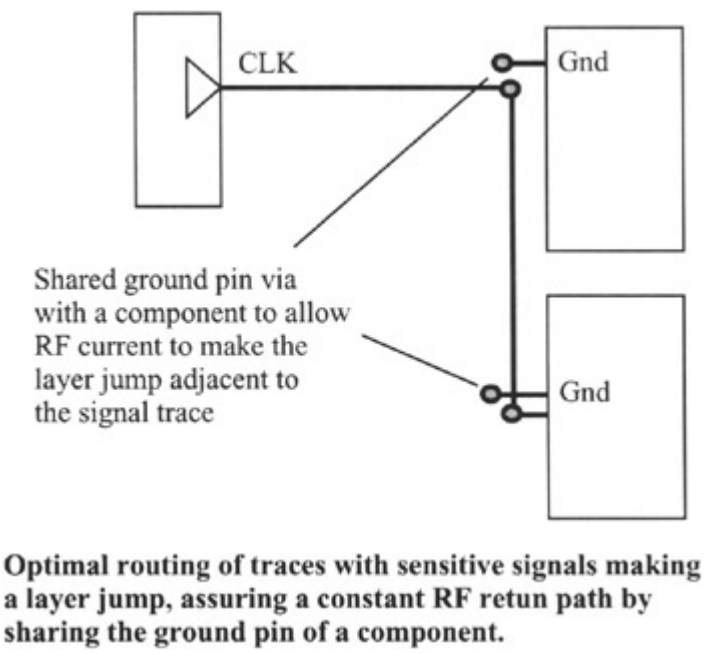
CLK
Gnd
Shared ground pin via
with a component to allow
RF current to make the
layer jump adjacent to
the signal trace
Gnd
Optimal routing of traces with sensitive signals making a layer jump, assuring a constant RF retun path by sharing the ground pin of a component.

Figure 4.16: How to route the first trace within a PCB.

[3]Use of ground vias was first identified and presented to industry by W.

Michael King. Ground vias are also described in [1 and 10].

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

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by Mark I. Montrose

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Recommend this title? yes no

4.10 CROSSTALK

4.10.1 Description of Crosstalk

Crosstalk is one important aspect of a layout that must be considered during the design cycle. It refers specifically to unintended electromagnetic coupling between traces, wires, trace-to-wire, cable assemblies, components, and other electrical components subject to electromagnetic field disturbance. These paths include PCB traces. This undesirable effect is associated not only with clock or periodic signals, but also with other system critical nets. Data, address, control lines, and I/O may be affected by crosstalk and coupling effects. Clock and periodic signals create the majority of problems and can cause serious functionality concerns (signal integrity) to other sections of the assembly.

Crosstalk between wires, cables, and traces affects intrasystem performance [6]. *Intrasystem* refers to both source and receptor being located within the same enclosure. A product must be designed to be self-compatible. Hence, crosstalk may be identified as EMI internal to a system that must be minimized or eliminated.

Crosstalk is generally considered a functionality concern (signal quality), for it causes a disturbance between traces. In reality, crosstalk represents RF energy coupled from a source trace to a victim trace. EMI-sensitive circuits may, however, also unintentionally couple their RF energy to other sections, including interconnects. I/O coupling can result in radiated or conducted EMI present within the enclosure, or it can cause functionality problems between circuits and subsystems.

For crosstalk to occur, three or more conductors are required. These three conductors are identified in Fig. 4.17. Two lines carry the signal of interest, and the third line is a reference conductor that gives the circuit the ability to talk (communicate) by capacitive or inductive coupling. If a two-wire system is provided, one of the wire pair is usually at reference potential while the other is differential. This prevents crosstalk from naturally occurring [6].

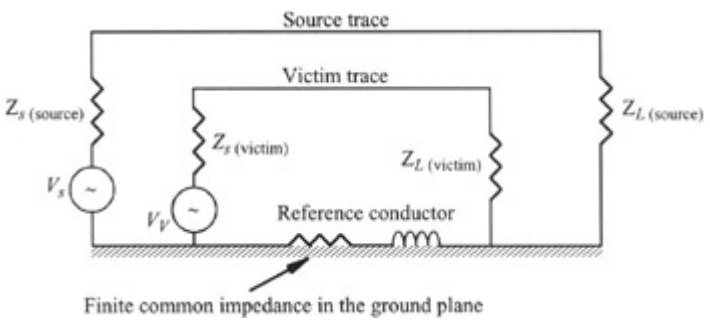

Figure 4.17: Three-conductor representation of a transmission line illustrating crosstalk.

Figure 4.17 illustrates coupling between two circuits due to the result of a nonzero impedance in the mutual reference conductor. This nonzero impedance is a prime reason to maintain a low-impedance path between connecting points.

Crosstalk involves both capacitive and inductive coupling. Capacitive coupling usually results when one trace lies on top of another trace. This coupling is a direct function of the distance spacing between the trace and an overlap area. Coupled signals may exceed design limits with a very

short trace route. This coupling may be so severe that overlapping parallelism should be avoided at all times. Capacitors allow RF energy to travel between two parallel plates through a dielectric. When a trace is physically located above or below another trace or a plane, a capacitive network is developed. Switching energy from one circuit will couple to the other, thus causing signal integrity concerns.

Inductive crosstalk involves traces that are physically located in close proximity to each other. This coupling results from expanding and contracting electromagnetic fields produced by switching currents in the trace. This coupling can be related to the primary and secondary winding of a transformer, where magnetic fields from one side of the transformer (primary) interacts with other windings (secondary) to transfer a signal of interest. This coupling analogy is the same between PCB traces and a typical transformer related to how field coupling occurs.

With parallel routed traces, two forms of crosstalk are observed: forward and backward. The signal that appears on the victim line at the source of the inducing line is referred to as *backward crosstalk*, whereas the signal observed at the received end of the victim trace is identified as *forward crosstalk*. Backward crosstalk is considered a greater concern than forward crosstalk. The high impedance in the circuit between source and victim trace will produce a high level of crosstalk. Figure 4.18 illustrates both forward and backward inductive crosstalk effects.

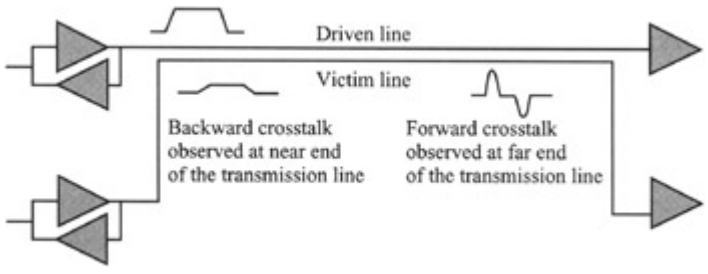

Figure 4.18: Forward and backward crosstalk effects.

The preferred method for preventing crosstalk must be determined during routing and layout in relation to cables, interconnects, and similar circuits subject to corruption. Inductive crosstalk can be controlled by increasing trace edge-to-edge separation between offending transmission lines or wires or by minimizing height separation distance of the traces above a reference plane.

Capacitive and inductive coupling can now be detailed (see Fig. 4.19). If a signal is sent from source-to-load, trace *A*-*B*, the signal will capacitively couple to the adjacent trace *C*-*D* only, providing the two lines are parallel to each other and are in close proximity. The larger the capacitance between the two traces (mutual capacitance), the tighter the coupling that occurs with electromagnetic energy transferred between the two. The coupled voltage on the victim trace, *C*-*D*, causes a current to flow from the "coupling point" toward both ends of the trace. The current going back toward the source, *C*, is backward crosstalk, whereas the signal traveling to the load, *D*, is forward crosstalk. The two traces also have mutual inductance between them, causing inductive coupling, L_m. If the output impedance of the driver, *C*, is normally low compared to the transmission line impedance, most of the backward crosstalk is reflected back toward the driver, *C*. Since a capacitor conducts RF energy (current) efficiently at high frequencies, the faster the edge rate, the greater the crosstalk.

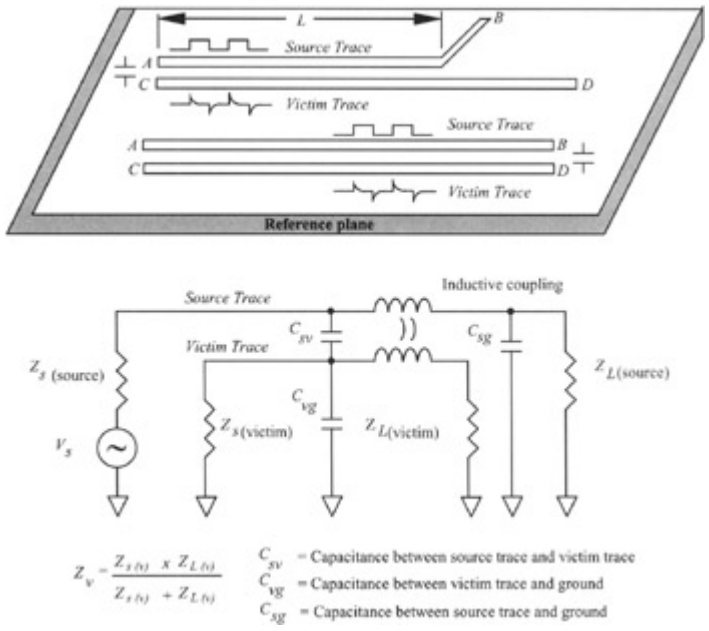

Figure 4.19: Fundamental representation of crosstalk.

4.10.2 Design Techniques to Prevent Crosstalk

To prevent crosstalk, the following design and layout techniques are useful during PCB layout:

1. Group logic families according to functionality. Keep the bus structure tightly controlled.
2. Minimize physical distance between components during placement.
3. Minimize parallel routed trace lengths.
4. Locate components away from I/O interconnects and other areas susceptible to data corruption and coupling.
5. Provide termination on impedance-controlled traces, or traces rich in RF harmonic energy.
6. Avoid routing of traces parallel to each other. Provide sufficient separation between traces to minimize inductive coupling effects.
7. Route adjacent layers (microstrip or stripline) orthogonal. This prevents capacitive coupling between adjacent layers.
8. Reduce signal-to-ground reference distance separation.
9. Reduce trace impedance and signal drive level.
10. Isolate routing layers that must be routed in the same axis by a solid planar structure (typical of backplane stackup assignments).
11. Partition or isolate high noise emitters (clocks, I/O, high-speed interconnects, etc.) onto different layers within the stackup assignment.
12. Provide a band-limiting filter on specific transmission lines to prevent RF frequencies from coupling between source and victim traces. This filter consists of a simple *RLC* resonant shunt circuit in series between the source trace and 0V-reference.

The best technique for preventing or minimizing crosstalk between parallel traces is to maximize separation between the traces or bring the traces closer to a reference plane. These layout techniques are preferred for long signals trace routing and high-speed parallel bus structures. Use of the *3-W rule* (next section) allows designers to comply with PCB layout requirements without having to implement elegant design techniques. This design technique does, however, take up physical real estate and may make routing more difficult.

When using mixed logic families, design rules must take into consideration coupling levels between parallel traces. Five percent coupling between TTL traces may be acceptable. However, if the victim trace is TTL to LVDS (low-voltage differential signaling), ECL, or PCI bus, 5 percent variation of signal transition for a MOS (metal-oxide-silicon) component may be too much. To make sure that intertechnology coupling is properly managed,

distance spacing must be calculated between similar logic families and between different technologies of component designs. When performing calculations for different technologies on the same routing layer, one must identify those traces that require one set of calculations and another set of dimensions for the other circuits. This information needs to be provided to the autorouter as a routing constraint. This is best achieved when a special list of net-classes is identified to the router. Various crosstalk configurations are shown in Fig. 4.20.

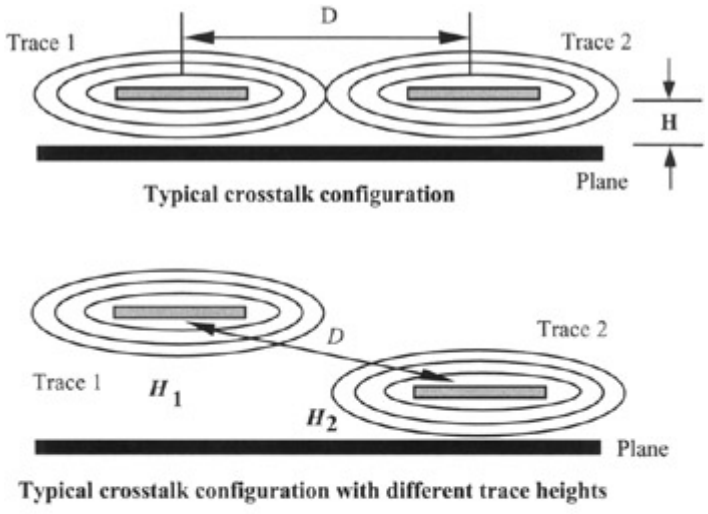

Figure 4.20: Calculating crosstalk separation.

Because of the current density distribution of the magnetic flux within a transmission line, the associated local magnetic field strength drops off with distance. An easy method to calculate trace separation is to use Eq. (4.24). This equation expresses crosstalk as a ratio of measured noise voltage to the driving signal. The constant *K* depends on the circuit rise time and the length of the interfering traces. This value is always less than one. For most approximations, the value of one is generally used. This equation clearly shows that to minimize crosstalk, we must minimize *H* and maximize *D* [10].

(4.24)
$$\text{Crosstalk} \approx \frac{K}{1 + \left(\frac{D}{H}\right)^2} = \frac{K(H)^2}{H^2 + D^2}$$

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For embedded microstrip, if the parallel traces are at different heights, the H^2 term becomes the product of the two heights, shown in Fig. 4.20 and Eq. (4.25). The dimension *D* becomes the direct distance between the centerline of the traces [10].

(4.25)
$$\text{Crosstalk} \approx \frac{1}{1 + \left(\frac{D}{H_1 * H_2}\right)^2}$$

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If traces are routed stripline between two reference planes, *H* must be determined using a parallel combination of heights to each plane, Eq. (4.26). (The numeric value of *n* refers to the trace number and is not a variable within the equation.)

(4.26)
$$H_{\text{total}} = \frac{Hna * Hnb}{Hna + Hnb}$$

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

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4.11 TRACE SEPARATION AND THE 3-W RULE

The *3-W rule* is used basically to minimize coupling between transmission lines or PCB traces. The rule states that *the distance separation between traces must be three times the width of a single trace measured from centerline to centerline*. Otherwise stated, *the distance separation between two traces, edge-to-edge, must be greater than two times the width of a single trace*. For example, a clock line is 6-mils wide. No other trace can be routed within a minimum of 12 mils (2 * 6 mils) of this trace, edge-to-edge. As observed, much real estate is lost in areas where trace isolation occurs. An example of the *3-W rule* is shown in Fig. 4.21.

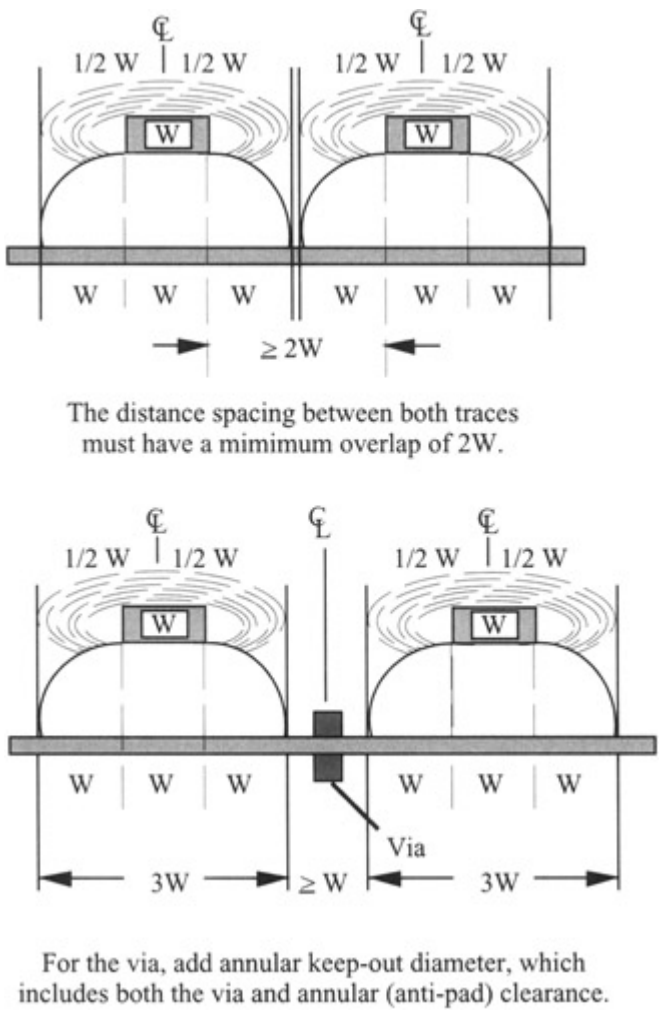

Figure 4.21: Designing with the 3-W rule.

The *3-W rule* is affected by the presence of a reference plane and the distance of the signal trace above that plane. The main item to note is that prevention of magnetic flux coupling to adjacent traces occurs in the horizontal axis. If a reference (return) plane is physically closer to the signal trace than the trace-to-trace spacing, the plane will minimize magnetic flux within the transmission line, thus enhancing performance over that of the *3-W rule*.

Note that the *3-W rule* represents the approximate 70% flux boundary at logic current levels. For the approximate 98% boundary, *10-W* should be used. These values are derived from complex mathematical analysis, which is beyond the scope of this book.

Use of the *3-W rule* is mandatory for *only* high-threat signals, such as clock, differential pairs, video, audio, the reset line, or other system critical nets. Not all traces within a PCB have to conform to *3-W* routing. It is important to determine which traces are to be classified as critical. Before using this design technique, it is important to determine exactly which

traces must be routed *3-W*.

As shown in Fig. 4.21, a via is located between two traces. This via is usually associated with a third routed net, and it may contain a signal trace that is susceptible to electromagnetic field disruption. For example, the reset line, a video or audio trace, an analog level control trace, or an I/O interface may pick up electromagnetic energy by either inductive or capacitive means. To minimize crosstalk corruption to the via, the distance spacing between adjacent traces must include the angular diameter and clearance of the via. The same requirement exists for the distance spacing between a routed trace rich in RF spectral energy that may couple to a component's breakout pin (pin escape) to this routed trace.

Use of the *3-W rule* should not be limited to clock or periodic signal traces. Differential pairs (balanced, ECL, and similar sensitive nets) are also prime candidates for *3-W*. The distance between paired traces must be *1-W* for differential traces and *3-W* from each of the differential pairs to adjacent traces. For differential pair traces, power plane noise and single-ended signals can capacitively, or inductively, couple into the paired traces. This can cause data corruption if traces not associated with the differential pair are physically closer than *3-W*. An example of routing differential pair traces within a PCB structure is shown in Fig. 4.22.

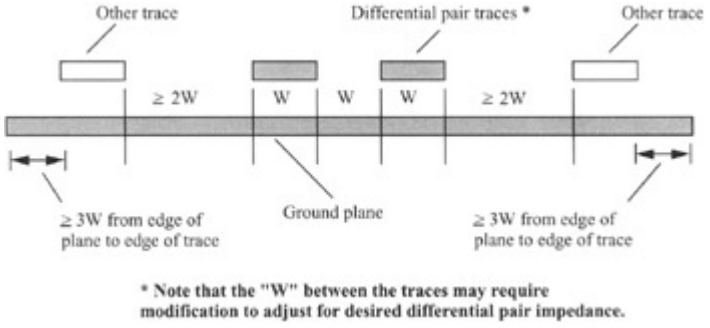
Other trace
Differential pair traces *
Other trace
≥ 2W
W
W
W
≥ 2W
≥ 3W from edge of plane to edge of trace
Ground plane
≥ 3W from edge of plane to edge of trace
* Note that the "W" between the traces may require modification to adjust for desired differential pair impedance.

Figure 4.22: Parallel differential pair routing and the 3-W rule.

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4.12 GUARD/SHUNT TRACES

Guard traces are traces at 0V-potential that surround clocks, periodic signals, differential pairs, or system critical (high-threat) nets from source to destination. Shunt traces are traces located directly above or below a high-threat transmission line that parallels the trace along its entire route. Both guard and shunt traces have unique applications, implementations, and drawbacks. Depending on functional requirements, one or both techniques may be used. It is up to the design engineer to select which technique is required for suppression of RF energy (flux cancellation/minimization). Guard and shunt traces have no effect in enhancing the signal integrity of the desired signal. If the purpose of using guard traces is to prevent crosstalk, or magnetic field coupling between adjacent traces, use of the *3-W rule* generally provides an adequate flux boundary, circumventing the usefulness of a guard trace.

Shunt traces are used when the sensitivity of a trace is critical, related to crosstalk corruption, or when a known amount of excessive RF energy will be present within a particular transmission line or trace. Routing a trace at 0V-potential parallel, or adjacent, to the signal trace allows for enhanced flux cancellation in differential mode. The shunt trace acts as an image plane and must be three times the width of the signal trace to fully capture flux that surround the trace. If the trace has an image plane on one side, at 0V-potential, and a shunt trace on the other side, also at 0V-potential, a partial coaxial transmission line structure is developed. If guard traces are provided with a shunt trace, a true coaxial transmission line exists. For many applications, implementing the use of guard traces in a stripline topology is a waste of time. A reason for this statement follows and becomes obvious when Fig. 4.23 is examined.

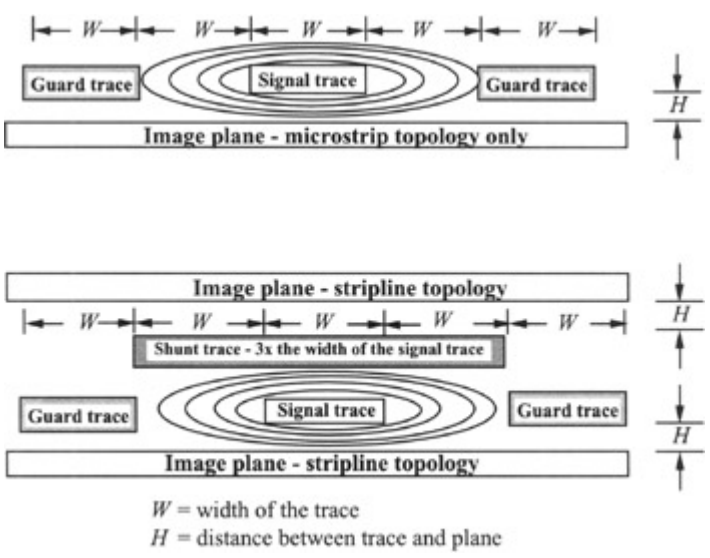

Figure 4.23: Shunt and guard trace configuration.

The RF field created from electromagnetic distribution within a signal trace is approximately *1-W*, or one width distance away from the trace, where *W* is trace width. Since field distribution is uniform around the trace, magnetic flux will be captured by the guard trace, shunt trace, or image plane, whichever one is *physically* closest to the trace.

Figure 4.23 is for illustrative purposes. Two examples will describe how and why guard and shunt traces either work or do not work within a stripline configuration.

1. The width of a trace (*W*) is 0.010 in. (0.25 mm). The distance spacing between traces is also 0.010 in. (0.25 mm), per manufacturing

requirements. If the distance spacing between signal trace *and* image (reference) plane (H) is 0.008 in. (0.20 mm), magnetic flux will see the image plane long before the guard trace observes this field. With close dimensional spacing, guard traces become useless. This is the primary explanation for why guard traces do not work well for some stripline configurations. If a guard trace is implemented as stripline to remove radiated RF energy developed within the transmission line, and the image planes located both above and below the signal trace *already* prevent RF energy from radiating to the environment, why use guard traces?

2. A different stackup assembly is now provided, with the same trace width (*W*) at 0.010 in. (0.25 mm). Separation distance (*W*) between the signal traces is also the same, at 0.010 in. (0.25 mm). Our new assembly now has a *greater* distance spacing between signal trace and the image plane (*H*) at 0.020 in. (0.5 mm). The distance spacing between guard trace and signal trace is now much less than the distance spacing between signal trace and image plane. For this particular application, the guard trace works as an enhanced alternate return path for the RF energy developed within the transmission line.

The important item to remember when defining mechanical constraints and constructional details of the PCB prior to placement and routing is the physical dimension between signal trace and image plane, or signal trace and guard or shunt trace. Whichever distance spacing is "closer" to the signal trace, enhanced suppression of RF energy will be achieved.

The primary function of both guard and shunt traces is to provide an alternate return path for RF currents to return to their source, if a solid image plane is not provided as in multilayer assemblies. If a single- or double-sided PCB is used, provisions for RF return currents will not exist in the same manner owing to lack of solid planar structures. If a guard trace is to be used in a multilayer assembly, this trace will provide a RF return path only if placed physically adjacent to the high-threat trace. The distance from signal trace to guard traces must be as close as can be manufactured.

If a two-layer (double-sided) PCB is used, with typical thickness spacing of 0.062 in. (1.6 mm), the physical distance between the signal trace, if routed on the top layer, and the ground plane, located on the bottom layer, is physically large. For all practical reasons, the RF return path is too far away to provide any significant amount of flux cancellation. For this application, guard traces are the designer's best friend only when routed as close as physically possible to the signal trace.

Guard and shunt traces are used for specific applications only. Applications are product specific and may not be required in most designs. The advantages and disadvantages of using both guard and shunt traces include the following:

1. *To enforce the 3-W rule*. When we increase the distance separation between traces, we minimize the amount of crosstalk that might develop between high-threat traces and other nearby components or traces. A guard trace forces the distance spacing between the source and victim trace to be much greater than if the guard trace was not present between the two. In addition, magnetic flux present within the transmission line containing RF energy will be captured by the guard trace, thus preventing crosstalk from occurring.

2. *To prevent common-mode RF coupling from a high-threat signal trace to other circuit traces* (minimize crosstalk). This application is one layout technique for preventing crosstalk, except instead of coupling magnetic flux between traces, common-mode currents are involved. If we prevent coupling, signal integrity is enhanced.

3. *To provide a low-impedance alternative RF return path and to minimize RF common-mode currents that may develop within the transmission line*. This is observed more with shunt traces than with guard traces. Chapter 2 discusses the need for RF currents to return to their source through the least amount of impedance. If a direct path is not provided, air becomes the path. Free space has an impedance of 377 ohms. A return path using a guard trace will provide much lower impedance to the RF current than no return path.

4. *To create an impedance-controlled, coaxial-based transmission line*

for specific nets. This coaxial type of configuration was shown in Fig. 4.23. Shunt traces perform best in multilayer boards (six or more layers). Shunt traces sandwich a high-threat signal trace between two separate reference sources (image plane and shunt trace). The advantage of using a shunt trace results from the skin effect of the currents flowing on the copper trace. There is no significant current flow inside the center of a trace. Placing a shunt trace directly above or below the signal trace provides for additional magnetic flux coupling of the trace, observed in Fig. 4.23.

5. *To enhance performance of low-technology stackup assignment related to signal integrity*. Guard traces are commonly found on single- and double-layer boards (e.g., those without power or ground planes). RF field capture occurs between a signal trace and reference plane through both capacitive and inductive coupling (including mutual inductance). This coupling removes common-mode currents and minimizes the signal-to-return loop area. Image planes provide tight RF coupling for return currents. Without a solid image plane on a single- or two-layer board, a guard trace provides this RF current return path.

If a shunt trace must be provided in a multilayer board, it must be placed immediately adjacent to the high-threat signal trace. Both ends of the shunt trace are then connected to the ground planes or 0V-reference. The shunt trace should not have voids in them—particularly those caused by vias. This is applicable "only" when stripline layers are provided between two planar structures. The width of the shunt trace must be at least three times the width of the signal trace. Additional via connections to the ground planes remove possible standing waves of RF currents projected onto the shunt trace [1]. Implementation of this scheme is rarely feasible and is impossible in many cases since the signal trace is routed on the horizontal axis, while the shunt trace is implemented on the vertical layer. This type of routing makes it nearly impossible to autoroute the PCB.

When using guard traces, the trace must be grounded at both source and destination. This ground connection must be as close as possible to the component. If the routing lengths of both the signal and guard trace are significant, multiple connections to the ground planes by vias, along the edges of the guard trace, are also required. These additional vias break up the resonant effects that occur from this potential "dipole" antenna.

When shunt or guard traces are connected to a 0V-reference, or ground, an interesting phenomenon is observed. An *LC* resonance can be developed (*L* from the trace and *C* from the distributed capacitance between trace and plane). Depending on the physical distance spacing between ground connections, sharp resonant impedances may be present. If any harmonic of the clock signal is at this exact resonant frequency, suppression of RF currents is made more difficult because the transmission line will create significant levels of RF energy. Should this occur, additional ground connections must be installed between 0V-reference and the shunt trace. What we are doing is changing the physical characteristics of the transmission line. The distance spacing of the ground vias should be altered to shift this resonant frequency away from where clock harmonics are anticipated to be observed.

When guard traces are used, the spacing between the guard and signal trace must be minimized to the smallest manufacturable distance. This distance must be maintained throughout the length of the route. Although the capacitive contribution of this spacing is minimal, suppression of RF energy could be significant.

When a guard trace is forced away from a signal trace due to vias or through-hole component leads in the routing path, this trace must be returned to normal as soon as the detour is cleared. Never locate anything between a signal trace and its guard trace. When two or more periodic signal or clock traces are routed side by side, they may "share" a common guard trace between them for only a short distance (see Fig. 4.24). All effort must be made to prevent routing two traces within the same guard trace if possible. Exceptions do exist, such as differential or paired signals. Differential pair traces usually do not require use of either guard or shunt traces.

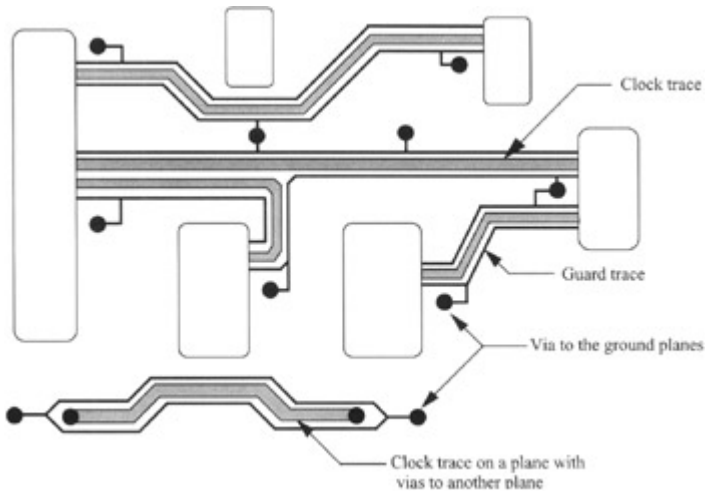

Figure 4.24: Guard trace implementation.

It must be restated here that "guard" traces are primarily effective on one- or two-layer circuit boards. On multilayer stackup assemblies, the flux boundary provided by the *3-W rule* will accomplish much of the benefit provided by guard traces, taking up significantly less real estate!

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Chapter 4 - Clock Circuits, Trace Routing, and Terminations

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4.13 TRACE TERMINATION

Trace termination plays an important role in ensuring optimal signal integrity as well as minimizing development of RF energy. To prevent impedance matching problems and provide higher quality signal transfer between circuits, termination may be required. Transmission line effects in high-speed circuits and traces must always be considered. If the clock speed is fast, for example, 100 MHz, and components are, for example, FCT series (2 ns edge rate being typical), reflections from a long trace route could cause the receiver to double clock on a single-edge transition. This is possible because it takes a finite time for the signal to propagate from source to load and return. If the return signal does not occur before the next edge transition event, functionality issues arise. Any signal that clocks a flip-flop is a possible candidate for causing transmission line effects, regardless of actual frequency of operation.

Termination absorbs excess or unwanted energy. Series termination affects this energy early in the transmission, while end termination absorbs it later. The topology chosen directs the energy to where it is needed, when it is needed. Excessive energy ends up going where it is not wanted, coming back later to cause functionality, EMI, and signal integrity problems.

Each source driver must have its respective output properly terminated. The most common forms of terminations are detailed in Fig. 4.25. An excellent discussion on using transmission line theory is found in Ref. [9, Chapters 3 and 7], and Ref. [1, 5].

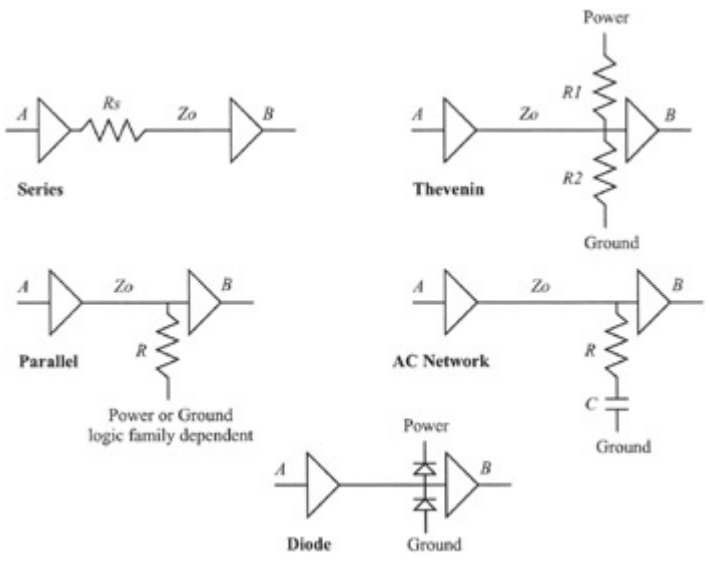

Figure 4.25: Common termination methods.

The need to terminate is based on several design criteria, the most important of which is the existence of an electrically long trace. When a trace is electrically long, or when the length exceeds one-sixth of the electrical length of the edge transition time, the trace requires termination. Even if a trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing.

Termination not only matches trace impedance and removes (reduces) ringing and reflections, but it may also slow down the edge rate transition of the clock signal if incorrect values are applied. Inappropriate termination may degrade the signal amplitude integrity to the point of nonfunctionality. Reducing either *dI/dt* or *dV/dt* within the trace will reduce the creation of RF currents generated by high-amplitude voltage and current levels.

The easiest way to terminate is to use resistive elements. Two basic

configurations exist, source and load. Several methodologies are available for these configurations, notably

1. Series termination resistor
2. Parallel termination resistor
3. Thevenin termination
4. AC termination (RC termination)
5. Diode termination
6. Differential signals

A summary of common termination methods is shown in Table 4.2, with the exception of differential signals; termination of differential, or paired signaling, is described at the end of this section.

Table 4.2: Termination Types and Characteristic Properties
Open table as spreadsheet

Termination Type	Added Parts	Delay Added	Power Required	Parts Values	Comments
Series	1	Yes	Low	$R_s = Z_o - R_o$	Good DC noise margin.
Parallel	1	Small	High	$R = Z_o$	Power consumption is a problem.
Thevenin	2	Small	High	$R = 2 * Z_o$	High power for CMOS.
AC (RC)	2	Small	Medium	$R = Z_o$ $C =$ 20–600 pF	Check bandwidth and added capacitance.
Diode	2	Small	Low	—	Limits overshoot; some ringing at diodes.

4.13.1 Series Termination

Series, or source termination, provides a mechanism whereby the output impedance of the driver and resistor matches the distributed impedance of the trace. The reflection coefficient at the source is zero. Thus, a clean edge transition signal is observed at the load. In other words, the resistor absorbs the reflections received from the load, preventing corruption to the first incident wave from the driver (Fig. 4.26).

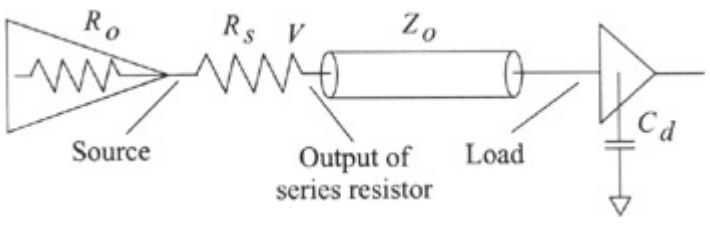

Figure 4.26: Series termination circuit.

Series termination is optimal when a lumped load or a single component is located at the end of a routed trace. The source output impedance, R_o, is usually less than Z_o, the loaded characteristic impedance of the trace. Loaded characteristic impedance refers to all loads that connect to the circuit, including capacitive overhead and inductive elements. A heavily loaded trace will lower the net impedance of the transmission line structure. The series resistor must be located directly at the output of the driver without use of a via between the component and resistor. The series resistor, R_s, is calculated by

(4.27) $$R_s = Z_o - R_o$$

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where R_s = series resistor

Z_o = characteristic impedance of the transmission line

R_o = output resistance of the source driver

For example, if R_o = 22 Ω, and trace impedance, Z_o = 55 ohms, R_s = 55 - 22 = 33 Ω. The series resistor, R_s, can be calculated to be greater than or equal to the source output impedance and lower than, or equal to, line impedance Z_o. Typical values are between 15 and 75 (usually 33) ohms.

4.13.2 End Termination

End termination is used when multiple loads exist within a trace route. Multisource drivers may be connected to a bus structure or daisy-chained. The last device on a routed net is where the end termination must be positioned.

To summarize:

1. The signal of interest travels down the transmission line at full voltage and current level without degradation.
2. The transmitted voltage level is observed at the load.
3. The end termination will remove reflections by matching the line impedance, thus damping out overshoot and ringback.

There is an optimal way to locate and route end terminators. This difference is shown in Fig. 4.27. Regardless of the method chosen, termination must occur at the "very end of the trace route." For purposes of discussion, the AC method is shown in this figure.

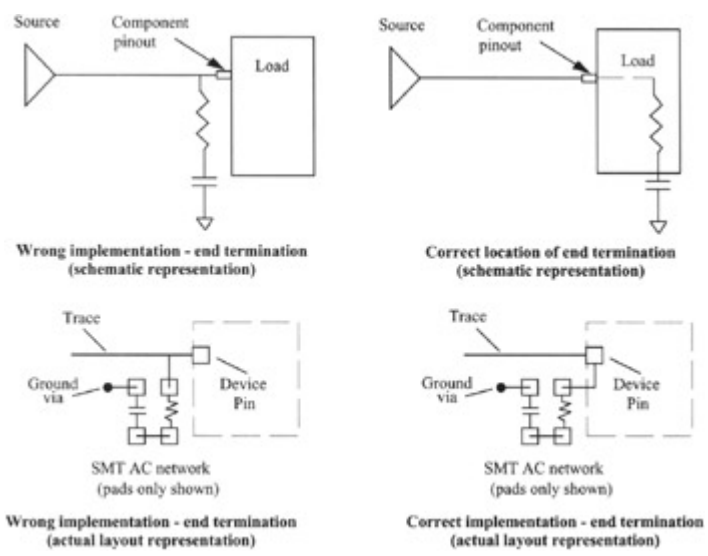

Figure 4.27: Implementing end terminators on a PCB.

4.13.3 Parallel Termination

For simple parallel termination, a single resistor is provided at the end of the trace route (Fig. 4.28). This resistor, R_p, must have a value equal to the required impedance of the trace or transmission line. For example, if the transmission line is 55 ohms, the value of R_p must be 55 ohms. The other end of the resistor is tied to a reference, generally ground. Parallel termination will add a small propagation delay to the signal due to the addition of the time constant, $\tau = Z_o C_d$, present in the network. This equation includes all capacitance within the transmission line structure and the input capacitance of the load. The total line impedance, Z_o, is the result of the termination resistor, line impedance, and source output impedance. The variable C_d in the equation includes both input shunt capacitance of the load and distributed capacitance of the trace.

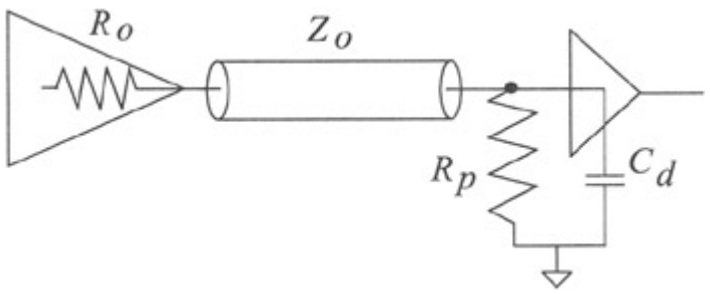

Figure 4.28: Parallel termination circuit.

A disadvantage of parallel termination is that this method consumes DC power, since the resistor is generally in the range of 50 to 150 Ω. In applications of critical device loading, or where power consumption is critical, for example, battery-powered products (notebook computers), parallel termination is a poor choice. The driver must source current to the load. An increase in drive current will cause an increase in DC power consumption from the power supply, which is an undesirable feature in battery-operated products.

Simple parallel termination is rarely used in TTL or CMOS designs because a large drive current is required in the logic HI state. When the source driver switches to V_{cc}, or logic HI, the driver must supply a current of V_{cc}/R to the termination resistor. When in logic LOW, no drive current exists. Assuming a 55 Ω transmission line, the current required for a 5V drive signal is 5V/55 Ω = 91 mA. Very few drivers can source that much current. The drive requirements of TTL demand more current in the logic LOW than logic HI. CMOS sources the same amount of current in both the LOW and HI logic states.

Simple parallel termination creates a DC current path to ground when the driver is at logic HI. Excessive power dissipation and V_{OH} degradation (noise margin) occur. Because a driver's output is always switching, DC current consumed by the termination resistor must exist. At higher frequencies, the AC switching current becomes the major component of the circuit. When using parallel termination, one should consider how much V_{OH} degradation is acceptable by the receivers.

When parallel termination is provided, the net result observed on an oscilloscope should be nearly identical to that of series, Thevenin, or AC, since a properly terminated transmission line should respond in the same way regardless of which method is used.

4.13.4 Thevenin Termination

Thevenin termination has one advantage over parallel termination. Thevenin provides a connection that has one resistor to the power rail and the other resistor to ground (Fig 4.29). Unlike parallel termination, Thevenin permits optimizing the voltage transition point between logic HI and logic LOW. When using Thevenin termination, an important consideration in choosing the resistor values is to avoid improper setting of the voltage reference level of the loads for both HI and LOW logic transition points. The ratio of *R*1/*R*2 determines the relative proportions of logic HI and LOW drive current.

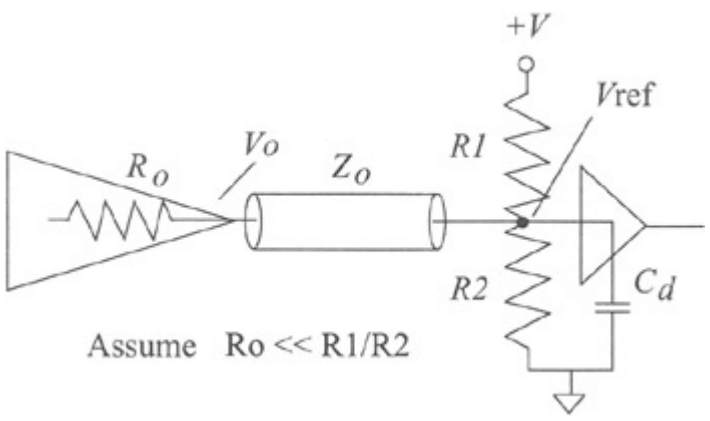

Figure 4.29: Thevenin termination circuit.

Designers commonly, but arbitrarily, use a 220/330 ohm ratio (132 ohms parallel) for driving bus logic. It may be difficult to determine the resistor ratio value, especially if the switch point for various logic families is different. This is especially true when both TTL and CMOS are used. A 1:1 resistor ratio (e.g., 110/110 ohms will create a 55-ohm value, the desired characteristic Z_o of the

trace) limiting the line voltage to 2.5V, thus causing an invalid transition level to exist.

The Thevenin equivalent resistance must be equal to the characteristic impedance of the trace. Thevenin resistors provide a voltage division. To determine the proper voltage reference desired, Eq. (4.28) is used.

(4.28)

$$V_{\text{ref}} = \frac{R_2}{R_1 + R_2} V$$

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where V_{ref} = desired voltage level to the input of the load

R_1 = pull-up resistor

R_2 = pull-down resistor

V = voltage source from the power rail

For the Thevenin termination circuit

$R_1 = R_2$:	The drive requirements for logic HI and LOW are identical. This setting may be unacceptable for most logic families.
$R_2 > R_1$:	The LOW current requirements are greater than the HI current requirement. This setting works well for TTL and CMOS devices.
$R_1 > R_2$:	The HI current requirements are greater than the LOW current requirement. This is a more appropriate selection for the majority of designs and logic families.

With these constraints, I_{OHmax} or I_{OLmax} must never be exceeded. This condition must be present, as TTL and CMOS sinks (positive) current in the logic LOW state. In the high state, TTL and CMOS source (negative) current. Positive current refers to current that enters a device, while negative current is the current that leaves the component. ECL logic devices source (negative) current in both logic states.

With a properly chosen termination ratio for the resistors, an optimal DC voltage level now will exist for both logic HI and LOW states. The advantage of using parallel termination over Thevenin is the parallel termination's use of one less component. If we compare the effects of parallel termination to Thevenin, both termination methods provide identical results. The signal within a transmission line will always be identical, regardless of which termination method is chosen.

4.13.5 AC Termination

The AC (also known as RC) termination method works well in both TTL and CMOS systems; it should be used only for clocks and never on data or address lines. The resistor matches the characteristic impedance of the trace (identical to parallel). The capacitor holds the DC voltage level of the signal. The source driver does not have to provide current to drive an end terminator. Consequently, AC current (RF energy) flows to ground during a switching state. A capacitor allows RF energy (which is an AC sine wave, not the DC logic level of the signal) to pass through. Although an additional propagation delay is presented to the signal due to the *RC* time constant, less power dissipation exists than parallel or Thevenin termination. From the viewpoint of the circuit, all end termination methods are identical. The main difference lies in power dissipation, with *AC* consuming far less power than the other two.

The termination resistor must equal the characteristic impedance, Z_o, of the trace, while the capacitor is generally very small (20–600 pF). The *RC* time constant must be greater than twice the loaded propagation delay (round-trip travel time). This time constant must be greater than twice the loaded propagation delay (2x) because a signal must travel from source to load and return. It takes one time constant each way for a total of two time constants. If we make the time constant slightly greater than the total propagation delay

within the routed transmission line, reflections will be minimized or eliminated. It is common to select a time constant that is three times the propagation delay of the round-trip signal. AC termination finds excellent use in buses containing similar layouts.

To determine the proper value of the resistor and capacitor, Eq. (4.29) provides a simple calculation, which includes round-trip propagation delay 2 * t'_{pd}.

$$\tau = RC \text{ where } \tau > 2 * t'_{pd} \tag{4.29}$$

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for optimal performance.

Figure 4.30 shows AC termination. The lumped capacitance (C_d plus C) affects the edge rate of the signal, causing a slower signal to be observed by the load.

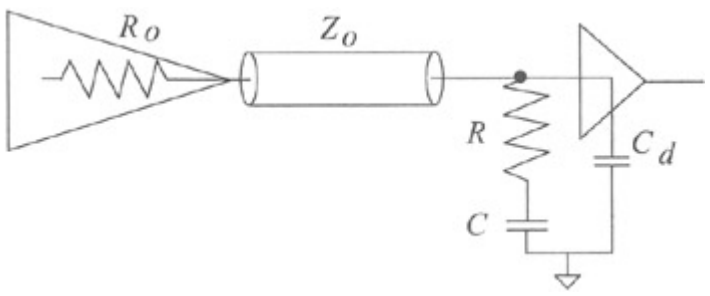

Figure 4.30: AC network circuit.

If the round-trip propagation delay, τ = 4 ns, RC must be > 8 ns. C can be calculated using the known round-trip propagation delay, employing the value of ϵ_r that is appropriate for the dielectric material provided and for the actual speed of propagation required.

4.13.6 Diode Network

This termination method is commonly used for terminating differential or paired networks. A schematic representation is shown in Fig. 4.31. Diodes are often used to limit over-shoot on traces while providing low-power dissipation. The major disadvantage of diode networks lies in their frequency response to high-speed signals. Although overshoots are prevented at the receiver's input, reflections will still exist in the trace, for diodes do not affect trace impedance or absorb reflections. To gain the benefits of both techniques, diodes may be used in conjunction with other methods discussed herein to minimize reflection problems. Another disadvantage lies in large current reflections that occur with this termination network. One should be aware, however, that when a diode clamps a large impulse current, this current can propagate into the power and ground plane, thus increasing EMI.

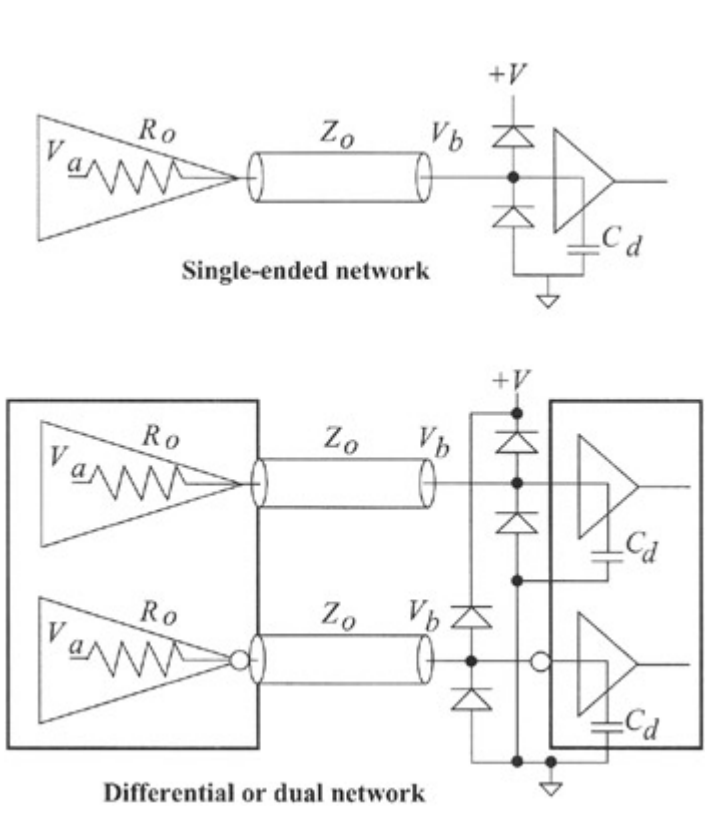

Figure 4.31: Diode termination—two configurations.

For certain applications, Schottky diodes are preferred. When using fast switching diodes, the diode switching time must be at least four times as fast as the signal rise time. When the line impedance is not well defined, as in

backplane assemblies, diode termination is convenient and easy to use. The Schottky diode's low forward voltage value, V_f, is typically 0.3 to 0.45V. This low-voltage level clamps the input signal voltage, V_f, to ground. For this high-voltage value, the clamp level is dependent on the maximum voltage rating of the device. When both diodes are provided, overshoot is significantly reduced for both positive and negative transitions. Some applications may not require that both diodes be used simultaneously.

The advantages of using diode termination include the following:

- Impedance matched lines are not required, including controlled transmission line environments.
- The diodes may be able to replace termination resistors if the edge rate is slow.
- Clamping action reduces overshoot and enhances signal integrity.

When using diode terminations, it is common to overlook the package lead-length inductance when modeling or performing computerized system analysis.

4.13.7 Differential or Paired Signaling

Differential signaling has been around for many years. With newer, high-speed components operating at a lower voltage swing level, this technique is becoming widely used as a means of minimizing power consumption and crosstalk coupling. Component technologies, such as LVDS, are now the preferred means of transporting very high data rate bit streams. Two areas of concern are mandatory for use with LVDS technology [3]: termination and impedance control. (Impedance control was discussed earlier in this chapter.)

A transmission line requires proper termination to eliminate reflections and enhance signal integrity. Various termination methods have been described for the single-ended transmission mode. Differential signaling requires an approach similar to the single-ended mode, with modifications.

Differential signaling requires that signal traces be routed on the same layer, either microstrip or stripline, and not a combination of both. This requirement is due to the velocity of propagation of the transmitted signal through the dielectric of the PCB. Signals routed microstrip will arrive at their destination faster than traces routed stripline. The longer the trace, the more significant this requirement becomes, especially if clock skew and timing at the differential receiver are critical.

Two propagation modes are present with differential signaling: differential mode and common mode. Both modes must be considered at the same time, according to the logic family selected. Differential-mode impedance is the value of the line-to-line resistor that will optimally terminate pure differential signals. Common-mode termination is the value of the signal trace to chassis ground. These types of configurations are illustrated in Fig. 4.32. Because a termination works for one propagation mode does not mean it will work for the other. Signals propagated differentially will also have a common-mode component. Sometimes both termination methods are required, depending on application and logic family.

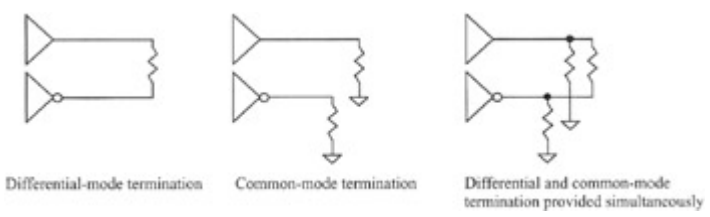

Figure 4.32: Differential- and common-mode signaling comparison.

The LVDS logic family requires a single differential-mode termination resistor, usually 100 ohms. Traces need to be approximately the same length to minimize signal skew. Common-mode RF energy is not present, since this logic family does not rely on a ground reference between source and load. This is the main benefit of using this logic family [3].

If the need to terminate two traces is required for any signal driven into them, a combination of both termination methods is permitted (Fig. 4.32). This

combination prevents reflections from propagating on the trace pair. To properly select a correct terminator, the following are recommended:

1. For common-mode signals, a line-to-line terminator (differential type) is invisible to the circuit. This means that no current flows through it. Termination to the transmission lines must be provided as a single-ended circuit, discussed earlier in this section.

2. For differential-mode signals, the line-to-ground terminators appear in series with each other across the line ends. Consequently, the line-to-line terminator should be the only additional resistance required to drop the trace impedance down to the differential impedance.

3. Resistor array terminators prevent reflections due to either differential-mode or common-mode signaling. In a true differential-mode environment, common-mode energy will not exist. Because differential-drivers are not perfect in their manufacturing, a small amount of common-mode energy will always be present.

Table 4.3 cites the advantages and disadvantages of various termination methods for paired signaling.

Table 4.3: Comparison of Termination Types for Paired Signals

➪ Open table as spreadsheet

Terminator Type	Advantages	Disadvantages
Differential resistor (across the differential lines)	Terminates differential signals. Requires only one component.	Does not terminate common-mode signaling or noise within the transmission line.
Common-mode resistor (resistor from each line to ground)	Terminates common-mode signals.	Does not terminate differential signals.
Resistor array	Terminates differential, common-mode, or any mix of signals.	Requires three resistors. May consume DC power.

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Chapter 5 - Interconnects and I/O

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Chapter 5: Interconnects and I/O

OVERVIEW

One of the more sensitive parts of a PCB in terms of EMI, ESD, and other forms of radiated and conducted susceptibility are I/O and related interconnects. These include serial and parallel ports, Ethernet, external storage drives, modems, video display, audio equipment, user interface (mouse, keyboard, joystick, scanners), and a wide range of other devices.

Most RF emissions in I/O circuitry are generated from

- Coupling of common-mode RF energy to I/O interconnects.
- Power plane switching noise coupling into I/O circuits and cables.
- Clock signals coupling to I/O cables through both conductive and radiated modes.
- Lack of data line filtering on signal traces (both common mode and differential mode).
- Improper connection of various ground methodologies (chassis, signal, digital, and analog).
- Use of unacceptable I/O connectors (plastic versus metal, or unshielded versus shielded).
- Ground potential difference between two circuits.

The I/O section generates as many problems with electromagnetic interference and susceptibility concerns as do clock signals—perhaps more. Proper component selection and placement minimize RF coupling that may occur for both conducted and radiated emissions. I/O must also be physically separated (electrically) on the PCB from high RF bandwidth components. If possible, separation from medium RF bandwidth circuits is also recommended, depending on the application.

An example of proper I/O implementation is to have metal connectors bonded to chassis ground through a low-impedance path, discussed in this chapter. This low-impedance path must be a 360° solid bonding of the metal housing to chassis ground. In addition, the designer must provide direct grounding of signal or chassis shield grounds immediately at the connector entrance point *without use of a pigtail* for circuits operating above 1 MHz.

I/O logic must be located as physically close as possible to the connector in order to minimize trace lengths and the risk that these signals will receive coupling from other circuits. Filtering is often required and is always placed between the driver and connector.

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5.1 PARTITIONING

Designing I/O circuits involves three areas of concern: functional subsystems, quiet areas, and internal radiated noise coupling.

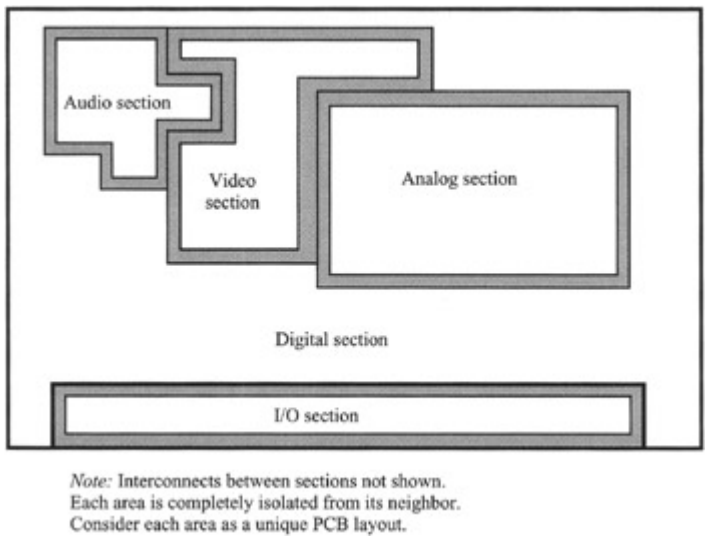
5.1.1 Functional Subsystems

I/O needs to be considered as different subsystems. Each circuit may be unique in its particular application. To prevent RF coupling between subsystems, partitioning may be required. A functional subsystem is a group of components and their respective support logic. Locating components close to each other minimizes trace length routing between circuits and optimizes functional performance. Engineers generally try to group components physically adjacent to each other, but for various reasons, it is sometimes impractical to do so. I/O subsystems must be treated differently during layout more than any other section of the PCB. This is performed through layout partitioning.

Layout partitioning enhances signal integrity by preventing high-bandwidth emitters (backplane interconnect, video devices, data interfaces, Ethernet controllers, SCSI devices, CPUs, and the like) from corrupting serial, parallel, video, audio, asynchronous/synchronous ports, floppy controller, front panel console displays, local area and wide area networks controllers, and so on. Each I/O must be conceived, designed, and treated as if the subsystems were separate PCBs.

5.1.2 Quiet Areas

Quiet areas are those sections that are physically isolated from digital, analog, and other functional areas. Isolation prevents noise sources located elsewhere on the PCB from corrupting localized, susceptible circuits. An example is RF energy within the power distribution network (digital) entering the power pins of analog, audio, video, and I/O interconnects (Fig. 5.1).



Note: Interconnects between sections not shown.
Each area is completely isolated from its neighbor.
Consider each area as a unique PCB layout.

Figure 5.1: Quiet area partitioning.

Every I/O port must be partitioned, or isolated, from the digital power/ground planes. Lower-frequency I/O ports may be bypassed with capacitors (usually 470 pF to 1000 pF) located near the connector to divert RF currents into the 0-V reference or chassis ground.

Trace routing on the PCB must also be controlled to avoid recoupling of internally generated RF currents into a cable shield, after filtering has been performed. A clean or quiet ground must be located at the point where interconnects leave the system. Both power and ground planes must be treated equally. RF return currents from switching devices to I/O components can inject high-bandwidth RF noise into cables and interconnects.

To implement a quiet area, use of a partition is required. This quiet area is implemented through the following:

1. I/O signals entering and exiting via an isolation transformer (Ethernet, telecommunications, or optical).
2. Data line filtered.
3. Filtered through a high-impedance common-mode inductor.
4. A ferrite material-based component.

The main objective of partitioning is to separate "dirty power and ground planes and other functional areas" from "clean or quiet zones and areas."

Another method of partitioning is also available. This method comprises a single-entry point between "dirty power/ground planes" and "clean or quiet zones." This single-entry point is called a bridge, described in the next section.

5.1.3 Internal Radiated Noise Coupling

Radiated RF coupling can occur between functional subsections. To prevent internal RF coupling (e.g., between internal peripherals and cables, cables to I/O connectors, and radiated RF currents from digital logic), a *fence* may be required. A fence is a metal barrier secured to the 0V-reference at intervals appropriate for the highest frequency ($\lambda/20$ wavelength) anticipated. The fence must be tall enough to prevent direct-line RF radiated coupling between components. A fence is similar to one side panel of a metal case that would normally encapsulate a circuit or component. This fence is physically similar to the standard bus bar used for power and ground distribution on single- or double-sided assemblies. At every ground location, it is important to bypass internally generated RF currents using a capacitor between the power and ground planes. One must select a capacitor with a self-resonant frequency appropriately calculated for optimal performance, not one with a value based on historical usage.

Determination must be made in advance if logic circuitry or subsections are candidates for both emissions of, and susceptibility to, internal radiated RF energy. Depending on the placement of components, relative to susceptible circuits or I/O connectors, potential coupling of internal radiated RF energy must be anticipated before routing traces or finalizing placement of components. Design provisions for future installation of a fence is recommended, since a fence is easily incorporated if mounting vias are provided. Actual implementation and use will be determined through functional testing. It is easier to add a fence to a PCB (addition to the bill of material) than to incorporate this fence in the artwork after the board has been manufactured.

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5.2 ISOLATION AND PARTITIONING (MOATING)

Isolation and partitioning refer to the physical separation of components, circuits, and planes from other functional devices, areas, and subsystems. Allowing RF currents to propagate to different parts of the board by radiated or conductive means can cause problems not only in terms of EMI, but also functionality.

CMOS and bipolar digital components create large transient current flow under three conditions:

1. Current flows directly from power to ground (internal power absorption).

2. Current flows from the power pin, through the chip, to the output pin (driving high, sourcing current to the loads).

3. Current flows into the output pin, through the chip, to its internal ground pin (driving low, sinking current from the loads).

The current flow pattern for item (1), for most small-scale (SSI) and medium-scale (MSI) integrated components, is by far the smallest of the three transient current conditions.

For situations (2) and (3), the chip creates large transient current loops that involve output pins, external loads, and the power and ground planes surrounding the chip. For example, suppose the chip is connected to a long, 50-ohm trace, and further suppose that the trace is routed on a layer adjacent to a reference plane. When the driver forces current into and out of that trace, an equal and opposite current flows on the reference plane, directly underneath the trace. This reaction current (or returning signal current) reenters the driver through either the power or the ground pin, depending on whether the driver is switching high or low, respectively.

A more general-purpose method of preventing digital currents from circulating into the analog ground plane would be the following (typical of layouts used with A/D converters in excess of 20 MHz with more than 8 bits). This design technique is called moating.

1. Partition the PCB. Divide into analog, digital, and I/O regions.

2. Isolate *all* plane layers along this partition line with absence of copper between regions. This absence of copper area is identified as a moat.

3. For power and ground planes, use a 0.010 in. (0.25 mm) minimum wide moat.

4. Tie analog ground and digital ground at *one* and *only one* point. This section of the ground plane will be the "bridge" that goes across the moat.

5. Locate the analog portion of analog components exactly in the middle across the bridge.

6. Permit no signals whatsoever to cross the moat in any location under any condition.

7. Ensure that any signals that must pass between the analog and digital sections travel only through the bridge, and do so on a layer adjacent to the bridge (maintain RF return current path).

8. Provide filters for analog power and phase lock loop circuits. This filter provides a digital noise-free analog power source.

Isolation is created by an absence of copper laminate on *all* planes. Absence of copper is created using a wide separation (typically a 10 mil minimum) from one section to another. In other words, an isolated area is an island in the middle of the board similar to a castle surrounded by a moat. Only those traces required for operation or interconnect can travel to this separate area. The moat serves as a keep-out zone for signals and traces unrelated to the area interface. Two methods exist to pass traces, power, and ground planes to this island, described in the following section. Method 1 uses isolation transformers, optical isolators, or common-mode data line filters. Method 2 uses a bridge. Isolation is also used to separate high-frequency bandwidth components from lower bandwidth circuits, in addition to maintaining low-EMI bandwidth I/O in terms of the RF spectrum.

When using this partitioning layout technique, a serious problem with implementation may occur. We have now divided the PCB into regions, digital and analog, providing one connection between them, the bridge. It is mandatory to exclude all other interground current pathways. No other connection must exist that would permit current to circulate between the digital and analog ground. If any current path exists, or if any other interground connection is present besides the one bridge, RF currents will circulate from digital ground, through the second interground connection (traveling across the moat) to the analog ground. This digital RF current will then return through the analog ground filter located across the bridge, returning to digital ground. This is exactly what we do not want.

5.2.1 Method 1: Moating

Method 1 involves use of an isolation transformer, optical isolators, or data line filters. The I/O area is thus 100% isolated from the rest of the PCB. A metal I/O connector, if provided, must be RF bonding to chassis ground through a low-impedance path, not to digital or isolated ground. Use of bypass capacitors from shield ground (or braid) of I/O cables to chassis ground is sometimes needed in lieu of a direct connection when required by the interface specification. Shield ground (or drain wire) refers to a discrete pin or wire that connects the internal drain wire of the I/O cable to the PCB.

There are two areas of concern for selecting components used in I/O circuits for isolation purposes:

1. Proper bandwidth filtering.
2. Peak surge voltage capabilities for electrostatic discharge protection.

For example, Ethernet or telecommunication circuits require use of an isolation transformer for compliance with interface specifications to physically isolate the network from the system (computer) in case an abnormal fault develops, thus maintaining network integrity. Common-mode data line filters, or chokes, may be used in conjunction with isolation transformers. Common-mode data line filters (usually toroidal in construction) may be used for both analog and digital applications. These filters remove undesired common-mode RF energy on signal traces exiting through I/O cables. If power and ground are required in the isolated area, (e.g., +5 VDC), the moat must be crossed with a ferrite bead for the power trace and a single solid trace for ground, three time the width of the power trace. The secondary short-circuit fuse (required for product safety) can be located on either side of the ferrite bead. Sometimes, decoupling is required to remove digital switching noise from filtered I/O power. Both power and ground trace are routed adjacent to each other to prevent potential RF ground loops that will be developed if both power and ground traces are located on opposite sides of the moat from each other (Fig. 5.2).

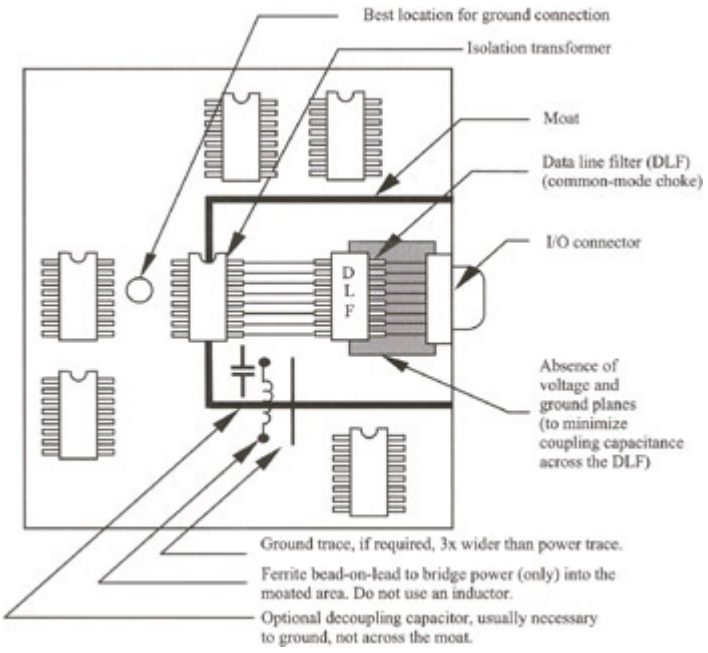


Figure 5.2: Using isolation with a moat—method 1.

There is an absence of copper area between the data line filter (DLF) and the I/O connector. This is a design technique not easily recognized. The concern for RF return current to have a return path physically adjacent to the signal line can be waived for this application. Common-mode RF energy is removed from the interface by the filter, preventing radiated RF energy from getting onto the cable. The cable interconnect provides a discontinuity in the return path, in addition to the fact that many cables provided by users are unshielded.

The DLF prevents RF energy from leaving the unit. What is not observed is what happens when an externally induced event occurs, such as ESD, conducted susceptibility, or an electrically fast transient burst. Externally induced energy is injected onto the signal cable. The cable brings the energy into the PCB. If an image plane is provided between the DLF and I/O interconnect, radiated coupling of high-energy levels of crosstalk may develop between signal lines and the plane. The plane will then recouple this energy to the input of the DLF, thus defeating its purpose and use. The item to remember is to keep undesired energy from coupling between filtered and unfiltered circuits. Mixing two circuits, at different potential levels, will result in serious functionality problems or permanent damage owing to component failure. This is useful only for a differential/balanced interface/line.

5.2.2 Method 2: Bridging in a Moat—Partitioning

Method 2 uses a bridge between a control section and isolated area. A bridge is a break in the moat at only one location, where signal traces, power, and ground cross (see Fig. 5.3). Violation of the moat by any trace not associated with the isolated area will cause serious problems. An RF loop current will be developed (Fig 5.4). RF currents must image back along their trace route, or common-mode noise will be generated between the two separated areas. Unlike Method 1, the power and ground planes are directly connected between the two areas.

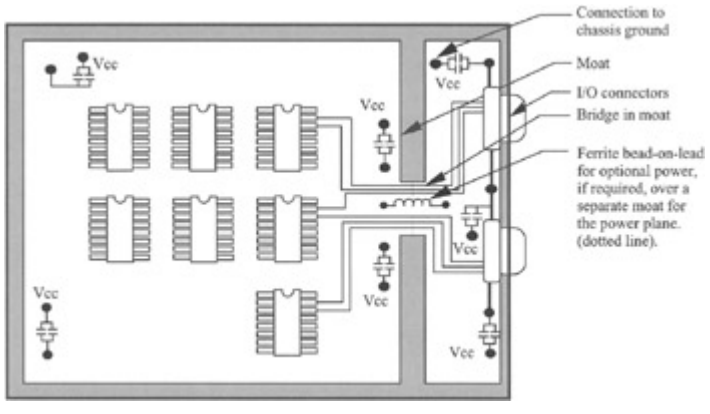


Figure 5.3: Partitioning I/O using a bridge in a moat—method 2.

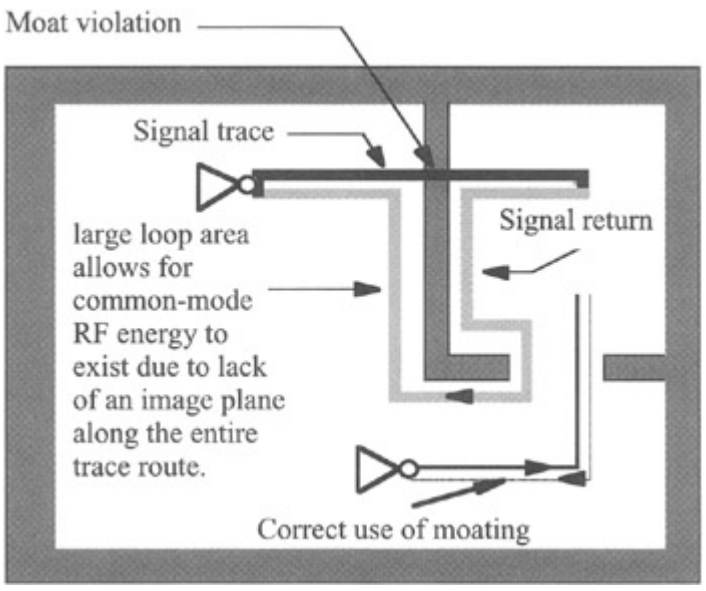


Figure 5.4: Violating the concept of moating.

Sometimes only the power plane must be isolated and the ground plane connected through the bridge. This technique is common for circuits where a common ground plane is needed, or separately filtered and regulated power is required. In this case, a ferrite bead is needed to bridge the moat for filtered power only. If analog or digital power is not required in an isolated area, this unused power plane can be redefined as a second ground plane, referenced to the main ground plane by vias within the isolated area.

When using bridging Method 2, both ends of the bridge should be bonded to chassis, or frame ground. This is highly recommended if multipoint grounding is provided in the chassis and system-level design. Grounding the entrances to the bridge performs two functions:

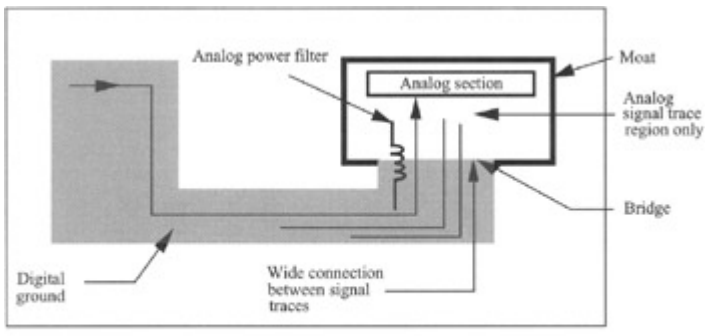
1. Grounding removes high-frequency common-mode RF components in the ground planes (ground-noise voltage) from coupling into the partitioned area.

2. Grounding minimizes eddy currents (for improved ground loop control) that may be present in the chassis or card cage. A much lower impedance path to ground is provided for RF currents (within the PCB) that would otherwise find their way to chassis ground through other paths, such as an I/O cable.

Grounding both ends of the bridge also increases electrostatic discharge immunity. If a high-energy pulse is injected into the I/O connector, this energy may travel to the main control area and cause permanent damage. This energy pulse must be sunk to chassis ground through a very low-impedance path to prevent component disruption or damage.

Another reason to ground both sides of a bridge is to remove RF ground-noise voltage created by voltage gradients that appear between the partitioned area and main control section. If common-mode noise contains high-frequency RF components, decoupling capacitors should be provided at each chassis ground stitch connection.

Figure 5.5 illustrates how traces are to be routed when using digital and analog partitions. Because power plane switching noise may be injected into the analog section from digital components, isolation and/or filtering is required, especially on the power plane. All traces that travel from the digital to analog section must be routed through a bridge. For analog power, a ferrite bead must be used to cross the moat. A voltage regulator may also be required. The analog power moat is usually 100% complete around the entire partition. Certain analog components will want analog ground to be referenced to digital ground, but only through a bridge, detailed in Fig. 5.5. Many analog-to-digital and digital-to-analog devices connect the "AGNDS" and "DGNDS" (indicated on the pin designation) together in the device lead frame. When such is the application of a partition, with one ground reference, digital signal currents will not return efficiently to their source, causing noise and EMI. AGNDS and DGNDS should be moated away from each other only when the circuit devices themselves provide AGND to DGND isolation.



Note: All signal traces must pass through this region only (bridge).
No signals are to pass over a plane void region (moat).
For the analog section, the power plane is 100% moated.
If a bridge is used for ground, both digital and analog ground will be at the same potential.

Figure 5.5: Digital and analog partitioning.

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Chapter 5 - Interconnects and I/O

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by Mark I. Montrose

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5.3 FILTERING AND GROUNDING

5.3.1 Filtering

Two types of filter configurations exist, capacitive and inductive (or their combinations). Different applications require one, the other, or both. Every I/O trace requires filtering, with exceptions permitted such as fiber optic and certain types of local area networks and telecommunication interfaces. Filter components will not be effective unless their placement is exactly adjacent to their entry point. One inch (2.54 cm) may be too far away. Capacitive bypass filtering is required to remove high-frequency RF currents on external I/O cable shields, in addition to inductive filtering for differential-mode RF current from logic devices and I/O interconnects.

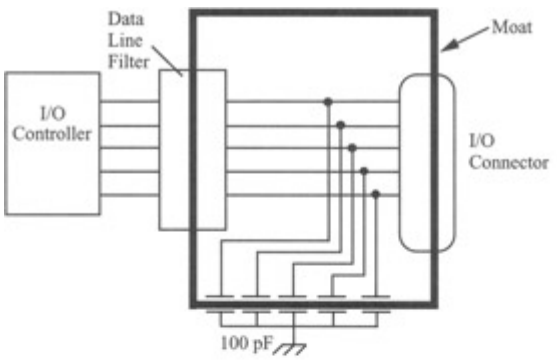
The differences among filter elements are as follows:

1. *Capacitors*. Used for bypassing RF energy from the shield of cables into a chassis ground; can also be used as part of an *LC* filter for operation at a particular frequency. The disadvantage of using capacitors is their sensitivity to high levels of voltage.

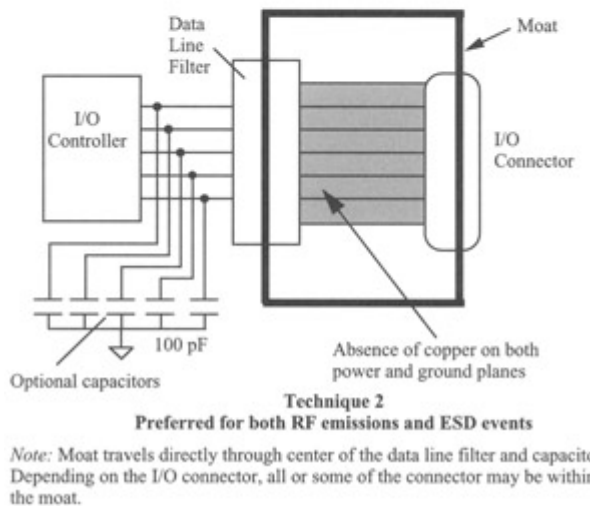
2. *Inductors*. Should never be used for filtering. Inductors placed within a circuit will slow down the rate of transient current flow, thus maximizing an induced event and possibly disrupting signal integrity. Another negative aspect of using inductors lies in the inductor's ability to cause a voltage potential difference between devices. A voltage potential difference between two sources, which are to be at the same potential, will cause common-mode current to develop, which is what we are trying to prevent in the first place.

3. *Ferrite material* (bead-on-lead, common-mode chokes, data line filter, or equivalent). Ferrite material is the optimal device to use for filtering. The bead absorbs high-frequency RF energy while allowing the DC signal of interest to pass without disruption. In addition to preventing internally induced RF energy from propagating to the outside world, the bead provides a high-impedance source at a frequency that most externally induced events occur, including ESD, fast transient, and conducted susceptibility. While keeping energy out, it also keeps energy from entering. Thus, this one component performs protection for both emissions and immunity. Note that ferrites are effective only at high frequencies, typically above 10 MHz.

For both radiated emissions and radiated susceptibility, if use of a capacitor is desired, the capacitor must be located directly at the connector entry point. The capacitor must be connected line-to-chassis, not line-to-line/return. A data line filter (common-mode choke or differential filter) must be positioned between the controller side of the signal trace and the connector, with the bypass capacitor between the two (Fig. 5.6, Technique 1). Filter capacitors are especially critical with keyboard, mouse, or external cables that may not be shielded. Their use as an effective filter device is significant, especially with requirements for regulatory compliance, especially immunity. ESD and RF fields are primarily a common-mode coupling event. Capacitors will effectively shunt the induced common currents to chassis. Any placement of the capacitor deeper inside the circuit will let the EMI enter further into the system.



Technique 1
Preferred for RF emissions



Technique 2
Preferred for both RF emissions and ESD events

Note: Moat travels directly through center of the data line filter and capacitors. Depending on the I/O connector, all or some of the connector may be within the moat.

Figure 5.6: I/O filtering methods.

For both radiated emissions and electrostatic discharge events, a different arrangement is required. The bypass capacitor should be located at the input side of the data line filter and not at the I/O connector, detailed in Technique 2 (Fig. 5.6).

These two design techniques are application dependent, as explained in the following section.

Technique 1. *Bypass capacitors at I/O connector*. Figure 5.6 shows filter capacitors located directly at the I/O connector. The capacitors are effective for both outgoing and incoming EMI. Selection of a bypass capacitor with a high self-resonant frequency is required for optimal performance. One must ensure that degradation of the signal edge does not occur beyond that required for proper operation of the signal. A 100-pF capacitor is commonly used for this application. This value is used because a larger value capacitor tends to round off the edges of a data signal beyond an acceptable level. With a rounded signal edge, performance degradation is expected.

In the case of an ESD event, voltage and current levels received may be extremely large in amplitude. International test specifications mandate a minimum voltage level for performance reasons. Surface mount capacitors used for RF emissions are usually rated 25 volts or less. Most capacitors will not only survive the ESD event, but will also protect the circuit from it. Transient surge protection devices are not always needed. Should an ESD event enter an I/O line, these capacitors may self-destruct. When this condition occurs, capacitive filtering for I/O lines no longer exist. This now leaves the unit noncompliant for both RF emissions and immunity purposes.

Technique 2. *Bypass capacitors between controller and data line filter*. International EMC requirements mandate that products must not only comply with radiated emission limits, but must provide a level of immunity to externally induced EMI. These externally induced RF fields may be a result of an ESD event, a fast transient burst or pulse, radiated or conducted fields from adjacent products, man-made RF energy (cellular telephones, pagers), or environmental events.

To prevent damage to low-voltage-rated surface mount capacitors, assuming a data line filter is provided, and still receive the benefit of bypassing, the capacitor must be located on the input side of the data line filter. This is shown in Fig. 5.6 (Technique 2). Use of π-filters is effective for this application. When an ESD event occurs, the pulse will first see a high-impedance source, the data line filter. The filter prevents this event from reaching control circuitry or other logic devices on the main part of the

PCB. ESD is essentially kept between the data line filter and I/O connector. If a circuit is sensitive to a particular frequency, a resonant *LC* filter can be designed. The data line filter must be replaced with an inductor for this application. Provisions should always be made for bypass capacitors during layout. Actual use will be determined through functional testing. In most cases, bypass capacitors will never be required, although the capacitor has been designed into the circuit and implemented in layout should use be required during functional testing.

To calculate the value of this bypass capacitor for use with an inductor, Eq. (5.1) is provided. A data line filter provides high-frequency attenuation of RF energy on signal lines but does not provide inductance that is part of a tuned filter equation.

(5.1)
$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{\left(\frac{1}{2\pi f_r}\right)^2}{L}$$

Get MathML

where f_r = resonant frequency of desired operation

L = inductance of the circuit including inductance of the capacitor leads (henries)

C = capacitance value (farads)

Inductive filtering is used in series with I/O signal lines to remove RF currents in the signal trace. Low-loss inductors make poor EMI filter elements. Use must be made of inductors that are RF energy absorbers. The problem with inductors is that they allow a voltage potential difference to be established between their leads. In addition, there is capacitance between all windings. Along with inductance of the device, the capacitance combination creates an *LC* filter that generally exacerbates the development of RF energy.

Chapter 8 presents detailed discussion on how to properly select a ferrite device (bead-on-lead, chip bead, toroidal shield bead, toroidal core, filter arrays, etc.) for suppression of RF currents, both common mode and differential mode.

When data line filters are used to bridge two areas, common-mode current is removed from the trace. Selection of the correct material type of data line filter is important because the ferrite material and construction operate at optimal performance within a specific range of frequencies (explained in Chapter 8). One manufacturer's filter or ferrite material may provide 30 ohms of impedance at 30 MHz and 300 ohms at 100 MHz. Another vendor's product (100% form, fit, function but with a different permeability value) may provide 15-ohm impedance at 30 MHz and 1000 ohms at 100 MHz. It should be verified before use that the permeability and composition of the ferrite material chosen is compatible with the intended range of frequencies to be suppressed. Vendor data sheets discuss this matter in detail.

Trace lengths between control logic and the I/O connector must be as physically short as possible. Filter components must always be located *directly* at the I/O connector and nowhere else. The same layout design techniques must be used for I/O signal traces as one would use for clock signals (discussed in Chapter 4).

5.3.2 Why I/O Cables and Interconnects Radiate

A decoupling capacitor is capable of driving a common-mode antenna, even though the capacitor may be located directly at the power and ground pins of a component. Large switching currents produced by components can develop a voltage potential difference between source and load. This voltage potential difference will drive two separate sections of the ground system against one another (as two halves of a dipole antenna). The common-mode voltage level of the antenna is increased by attempting to eliminate the voltage-driven mechanism through use of a decoupling capacitor. This capacitor is provided by the cable (interconnect), which is then connected to the driven element (signal trace), referenced to a return plane. The length of the differential-mode loop is increased as a result of the parasitic capacitance within the connector physically located distant from the source component. An increase in loop inductance will occur (source to I/O capacitor); hence, an increase in voltage drop is observed along the return conductor [2]. This configuration is illustrated in Fig. 5.7.

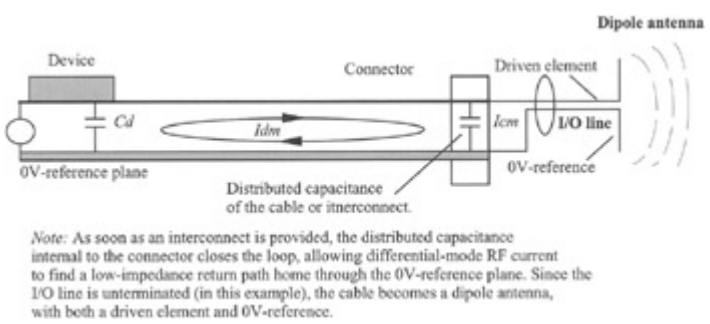

Dipole antenna
Device
Connector
Driven element
Cd
Idm
Icm
I/O line
0V-reference plane
Distributed capacitance
0V-reference
of the cable or itnerconnect.
Note: As soon as an interconnect is provided, the distributed capacitance
internal to the connector closes the loop, allowing differential-mode RF current
to find a low-impedance return path home through the 0V-reference plane. Since the
I/O line is unterminated (in this example), the cable becomes a dipole antenna,
with both a driven element and 0V-reference.

Figure 5.7: How common-mode energy gets developed on an interconnect cable.

With a voltage potential difference between a source and load, an optimal condition exists for driving a dipole antenna. The greater the potential difference, the greater the radiated emission.

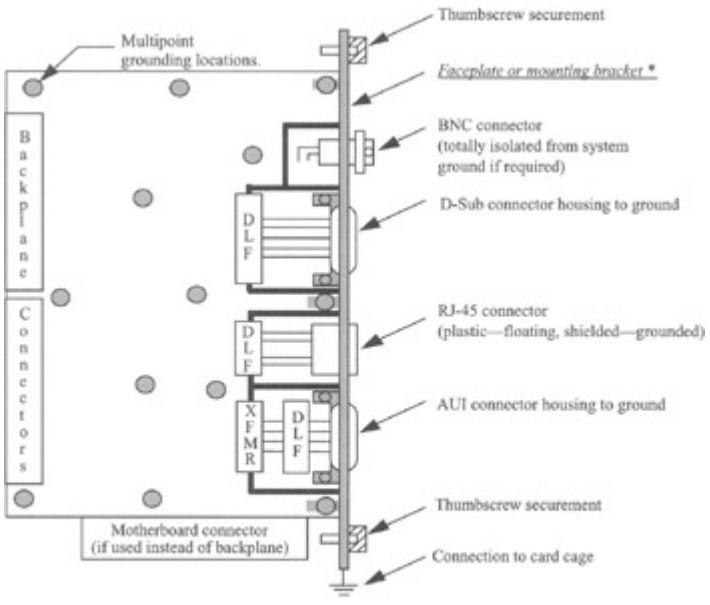
5.3.3 Grounding (I/O Connector)

For systems that are low-frequency and must use single-point grounding, this section is not applicable. For low-frequency products, a low-impedance connection between logic ground and chassis ground may not only cause electromagnetic interference, but may also prevent proper functionality of the circuit. This is especially true for audio circuits that are devoid of digital processing.

For a circuit to qualify as low-frequency, which is very difficult to define, to the extent that it also qualifies for single-point grounding, the combination of signals levels, packaging technology, and all operating frequencies must be such that transfer currents to the case (or external surfaces) through a distributive transfer impedance will be insignificant in comparison to the operative signal levels or the desired EMC criteria.

For products using multipoint grounding, this section is applicable whenever an I/O interface is implemented. Most modular PCBs contain a mounting bracket, faceplate, bulkhead connector, or a securement means between control logic and the outside world. This securement may contain various I/O connectors, or it may be a blank filler panel (EISA/ISA/PCI adapter bracket). This bracket must be RF bonded by a low-impedance metal-to-metal path directly to chassis ground. This bracket grounding may also be bonded to logic ground if the circuit allows for a direct connection at chassis potential, application specific.

For products that require extensive use of internal grounding, provision must be made for multiple connections from the 0-V reference planes of the PCB to the I/O bracket, or equivalent means of securement if the design permits this type of grounding. Multiple ground points redirect RF energy between ground locations and between opposite ends of the PCB. The better the grounding, the more sourcing of RF currents to chassis ground, minimizing disruption or electromagnetic interference. Figure 5.8 shows how to secure a mounting bracket for both chassis and logic ground. All I/O areas are isolated from the control logic by moats to prevent coupling of RF energy from digital circuits to adjacent I/O or the external environment.



*The mounting bracket is bonded (grounded) to the PCB as indicated in multiple locations.
The faceplate is also secured to the main chassis ground via thumbscrews or by other means.
Note the location of the ground points on the board to minimize ground loops.

DLF refers to data line filter.

Figure 5.8: Multipoint grounding of I/O faceplate or bracket.

Chapter 5 - Interconnects and I/O

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5.4 LOCAL AREA NETWORK I/O LAYOUT

Local area networks (LANs) and wide area networks (WANs) require careful attention during layout to allow compliance to international interface and emission requirements. The most commonly used LANs are Ethernet, Token Ring, FDDI (Fibre Distributed Data Interface), Wireless and Broadband. A sample listing of these specifications includes

ISO/IEC 8802.3	*Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications (Ethernet)*.
ISO/IEC 8802.5	*Token Ring Access Method and Physical Layer Specifications*. Subsections include STP (Shielded Twisted Pair), UTP (Unshielded Twisted Pair), and Fiber Optic.
ANSI X3.166	*Fibre Data Distributed Interface (FDDI)—Token Ring Physical Layer Medium Dependent (PMD)*.

Ethernet has different interface formats, each with a different front-end connector and design considerations. The most widely used Ethernet protocols are listed here. This list is not intended to be comprehensive, but only to illustrate variations within one type of LAN: Ethernet.

1.	10Base-10, 10Base-5	(10/5 MHz, AUI—Coax)
2.	10Base-2	(10 MHz, Thinnet—Coax)
3.	10Base-T	(10 MHz, RJ-45—twisted pair, shielded or unshielded)
4.	10Base-F	(10 MHz, FOIRL—Fiber Optic)
5.	10Base-FL	(10 MHz, FL—Fiber Optic)
6.	100Base-TX	(100 MHz, 100Base-T using two pairs of Category 5 UTP cable)
7.	100Base-T4	(100 MHz, 100Base-T using four pairs of Category 3, 4, or 5 UTP cable)
8.	100VG-AnyLAN	(100 MHz, using Category 3, 4, or 5 UTP, STP cable and fiber optic)
9.	Gigabit Ethernet	(Copper or fiber optics)

Telecommunication circuits also have various formats, each with a unique interface requirement. A sample listing includes T1, ISDN, D3, OC3, E1, E3, and the like.

The recommended design implementation for typical interconnects is illustrated in Figs. 5.9 to 5.12, which show a number of similarities. The layout concept and implementation merit close observation. Specific design details are left to the designer and will differ based on specific implementation requirements for each application. Typically, the order of component layout from the controller is: isolation transformer/wave shaping

circuit, data line filter, and I/O connector.

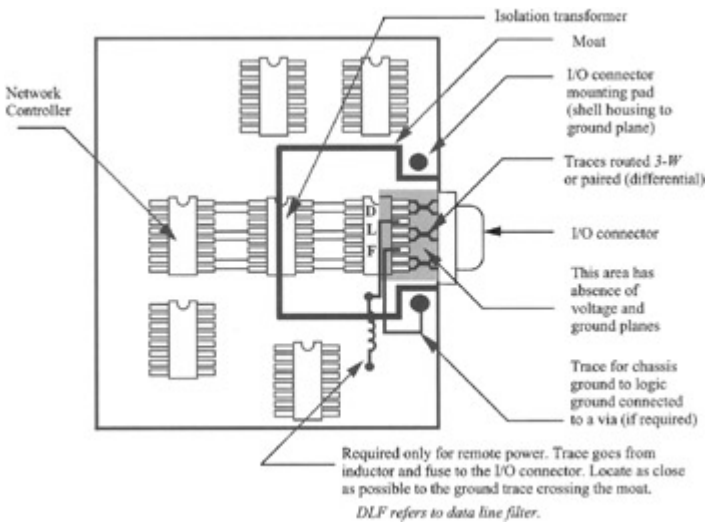
Isolation transformer
Moat
Network Controller
I/O connector mounting pad (shell housing to ground plane)
Traces routed 3-W or paired (differential)
D
L
F
I/O connector
This area has absence of voltage and ground planes
Trace for chassis ground to logic ground connected to a via (if required)
Required only for remote power. Trace goes from inductor and fuse to the I/O connector. Locate as close as possible to the ground trace crossing the moat.
DLF refers to data line filter.

Figure 5.9: Suggested layout for network and telecommunication interfaces.

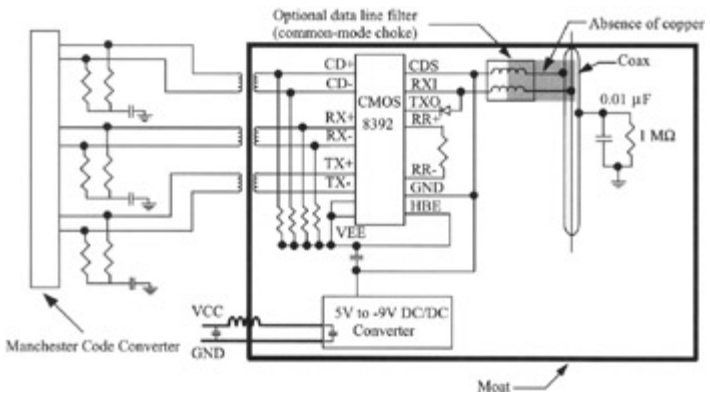

Figure 5.10: Suggested layout for coaxial based interconnects.

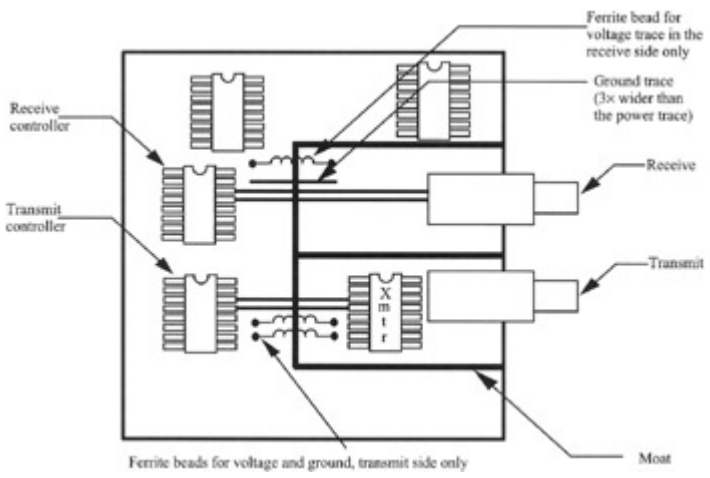
Ferrite bead for voltage trace in the receive side only
Ground trace (3× wider than the power trace)
Receive controller
Transmit controller
Receive
Transmit
X m i r
Moat
Ferrite beads for voltage and ground, transmit side only

Figure 5.11: Suggested layout for fiber optic interconnects.

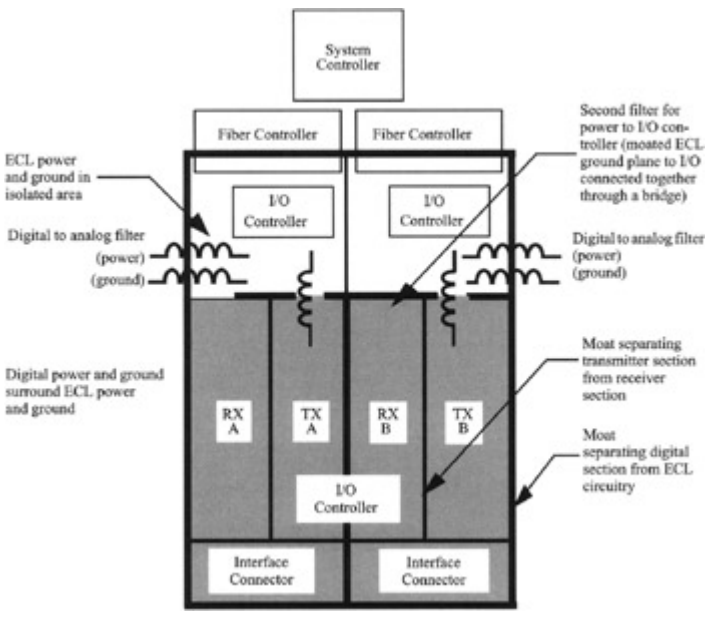

Figure 5.12: Suggested layout for a sophisticated fiber interface.

The recommended layout topology shown in Figs. 5.9 through 5.12 has been proven to allow compliance with International Class B emission requirements. Proper design of the interface is not the total solution for electromagnetic interference compliance. All other areas discussed in this book are still required, especially trace routing, proper selection of components and their placement, correct I/O isolation and filtering, optimal decoupling, and other design and layout techniques.

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5.5 VIDEO

Printed circuit boards with video require careful attention to impedance control, filtering, and grounding. For analog monitors, the slowest slew rate signal possible from the video generator is required. A passive filter must be installed between the video generator and I/O connector. Locate the filter immediately adjacent to the connector with minimal lead inductance. Manufacturers of video controllers generally prescribe a recommended way to layout the design, including selection of discrete components. For analog monitors, maintain constant trace impedance of the three RGB signals (red, green, and blue), along with both horizontal and vertical sync traces. These layout requirements prevent reflections from being developed owing to a potential transmission line impedance mismatch in the system and interconnect cable.

Two major concerns exist when performing a video layout: trace impedance and power purity. Trace impedance between the video generator and I/O connector must be matched to the video monitor for optimal performance. A typical PCB has trace impedance in the range of 55 to 65 ohms. Video requires 75 ohms, hence, an impedance mismatch will be present if a standard line width is used. For very dense, multilayer PCB assemblies, trace routing must occur over an area identified as an absence of copper section directly under the 75 ohm RGB circuitry to alter trace impedance of specific signals. This absence of the copper area (plane) forces the signal traces to be impedance referenced to a plane at a greater distance away, increasing overall impedance. This absence of copper area also prevents digital power plane noise from corrupting low-voltage level analog signals. A design technique to maintain impedance control is to alter the physical width of the trace on each routing layer in order to maintain a desired impedance throughout the trace route. Referencing a trace to a plane at a distance farther away within the stackup is how one can route a trace with a different impedance value than other traces with the same width on the same routing layer (Fig. 5.13).

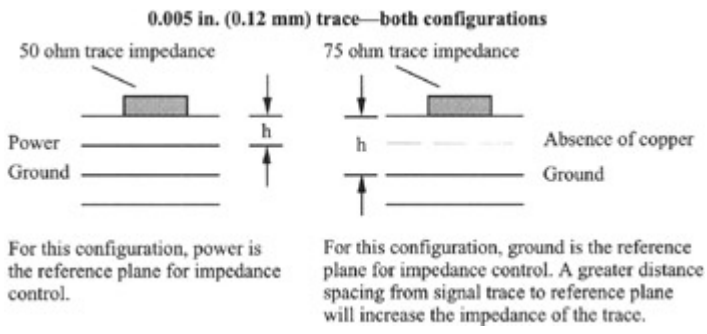
0.005 in. (0.12 mm) trace—both configurations
50 ohm trace impedance
75 ohm trace impedance
Power
Ground
h
h
Absence of copper
Ground
For this configuration, power is the reference plane for impedance control.
For this configuration, ground is the reference plane for impedance control. A greater distance spacing from signal trace to reference plane will increase the impedance of the trace.

Figure 5.13: Routing 75-ohm traces on a 50-ohm stackup assembly.

Most video systems require 75 ohm impedance. This higher impedance is required only from the *output* of the video generator to the I/O connector. Thus, the distance spacing of the routing layer to the reference plane between the controller and connector must be at a constant 75 ohm impedance for *all* analog traces within this area. Altering the width of the trace may also be required when the trace has to traverse through a via to another routing plane, which itself has a different impedance value. A trace width change is applicable when a signal layer is referenced to an alternate image plane. (Impedance control of microstrip and stripline layers is discussed in Chapter 4.)

One must maintain constant trace impedance for video signals routed on all layers from controller to connector. If this trace is routed 100% in the same signal plane, adjacent to a solid reference plane (tightly coupled), design techniques for alternating the trace width for each routing layer of the PCB for impedance control are not required.

With regard to power purity, a filtered isolated power source referenced to noisy (digital) power through a ferrite bead is required. Adequate decoupling must also be present for both the digital and analog side of the ferrite bead. A second ferrite bead for analog ground may be required (discussed next). All video and analog traces and their respective components must be located exclusively in the analog section. Proper component placement prevents digital switching noise from corrupting analog components. When designing isolation for analog with a moat between analog and digital, the *20-H* rule is required only for the analog power plane, shown in Fig. 5.14.

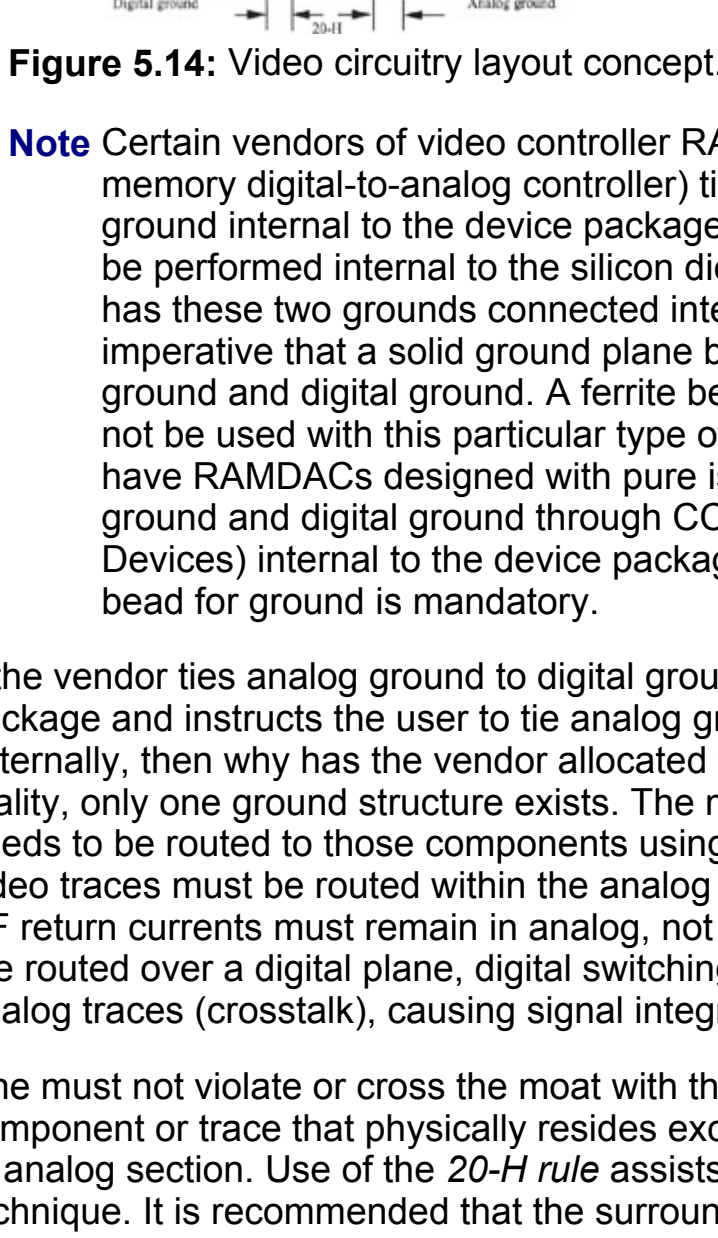
20-H spacing.
Power plane physically
smaller than ground plane
Separate partition for analog power and ground
VDD
GND
AVDD
AGND
Video Controller
R
G
B
APOWER and AGND Plane
AGND Plane
Digital signal traces to video controller
Digital logic and control circuitry
50 ohm traces
75 ohm traces
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Digital traces
Analog traces
Dead zone
Digital ground
Analog ground
Digital power
Analog power
Moat
Layer 2 (dead zone), nothing exists (no plane or traces). Provides for 75-ohm impedance traces on a 50 ohm PCB. Moat exists on only the five upper planes. Layer 5 (dead zone) keeps digital traces from corrupting the analog power plane.
Traces in this area at 75 ohms
50 ohm trace section
Analog section
Digital section
Closeup of I/O filters from controller to connector. Note that the filter components are located directly at the connector, away from the controller.
Note: If the AGND and DGND are common internal to the video controller (RAMDAC), then use only "one" ground plane. Do not isolate analog ground from digital ground! Certain vendors of RAMDAC controllers tie analog ground to digital ground inside the package. Other vendors have separate analog "and" digital grounds.
Ferrite bead
20-H

Figure 5.14: Video circuitry layout concept.

Note Certain vendors of video controller RAMDACs (random access memory digital-to-analog controller) tie analog ground to digital ground internal to the device package. This connection may also be performed internal to the silicon die. If the RAMDAC chosen has these two grounds connected internally together, then it is imperative that a solid ground plane be used for both analog ground and digital ground. A ferrite bead for ground pins should not be used with this particular type of RAMDAC. Other vendors have RAMDACs designed with pure isolation between analog ground and digital ground through CCD (Charged Coupled Devices) internal to the device package. For these parts, a ferrite bead for ground is mandatory.

If the vendor ties analog ground to digital ground *internal* to the device package and instructs the user to tie analog ground to the digital partition externally, then why has the vendor allocated the pin name as AGND? In reality, only one ground structure exists. The moat for the analog section needs to be routed to those components using filtered "analog" power. "All" video traces must be routed within the analog section, and their respective RF return currents must remain in analog, not digital. If the analog traces are routed over a digital plane, digital switching noise may couple to the analog traces (crosstalk), causing signal integrity concerns.

One must not violate or cross the moat with the placement of "any" component or trace that physically resides exclusively in either the digital or analog section. Use of the *20-H rule* assists in implementing this technique. It is recommended that the surrounding planes be at ground reference rather than voltage to minimize crosstalk between traces. This is shown in Fig. 5.14 for a multilayer stackup. For two-sided boards, the same

guidelines apply but with extra attention given to component placement and trace routing to prevent coupling noise between analog and digital sections. The discrete video filter components must always be located adjacent to the I/O connector, with minimal trace length routing possible.

Certain analog monitors use a coax from the I/O connector to the monitor. The braid, or shield, of the coax is not an RF shield but a video signal return path. This braid (shield) therefore cannot be RF bonded to chassis ground; rather it must be connected directly to the video return logic. Provision must always be made for an AC shunt using a bypass capacitor between the braid (shield) of the coax and system chassis ground. The shunt capacitor removes RF currents that may exist on the coax shield without affecting the signal integrity of the transmitted signal.

RF energy on a braid travels on the basis of skin effect. The inside portion of the braid carries the video return signal, whereas the outside portion of the braid carries RF energy. Because of the propagation mode of the electromagnetic wave within a transmission line, both RF and low-frequency energy will be present simultaneously. For this reason, the bypass capacitor is effective in removing unwanted high-frequency RF energy, while letting the desired low-frequency DC signal to pass undisturbed.

For PCBs with digital mode video interface, data line filters, or their equivalent, must be used only on high-threat signals. Constant trace impedance is mandatory at all times, taking into consideration layer jumping. The output portion of the video generator to the I/O connector must be located in an isolated (quiet) area (discussed earlier). RF ground (bond) the metal I/O connector and cable shield directly to chassis ground immediately at the exit point, if the cable braid (shield) *is not used* as signal return. If the I/O connector contains video return, then design requirements mandate isolation. Under this condition, a bypass capacitor is required to divert RF energy on the braid to chassis ground. Externally induced RF energy is not to be allowed to corrupt the video circuitry once it enters the system.

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5.6 AUDIO

Printed circuit boards with audio generally require three separate partitioned areas: digital, analog, and audio. This multilevel partitioning is applicable only for a four- or more layer stackup, and it is impossible for two-layer assemblies. Most two-layer PCBs do not implement moats, for it is impossible to use split plane technology when solid reference planes do not, and cannot, exist.

The analog section must be isolated from the digital area using a bridge or moat. An example of this multilevel partitioning is shown in Fig. 5.15. The concept used for partitioning analog and digital is similar to a video layout, discussed in the previous section.

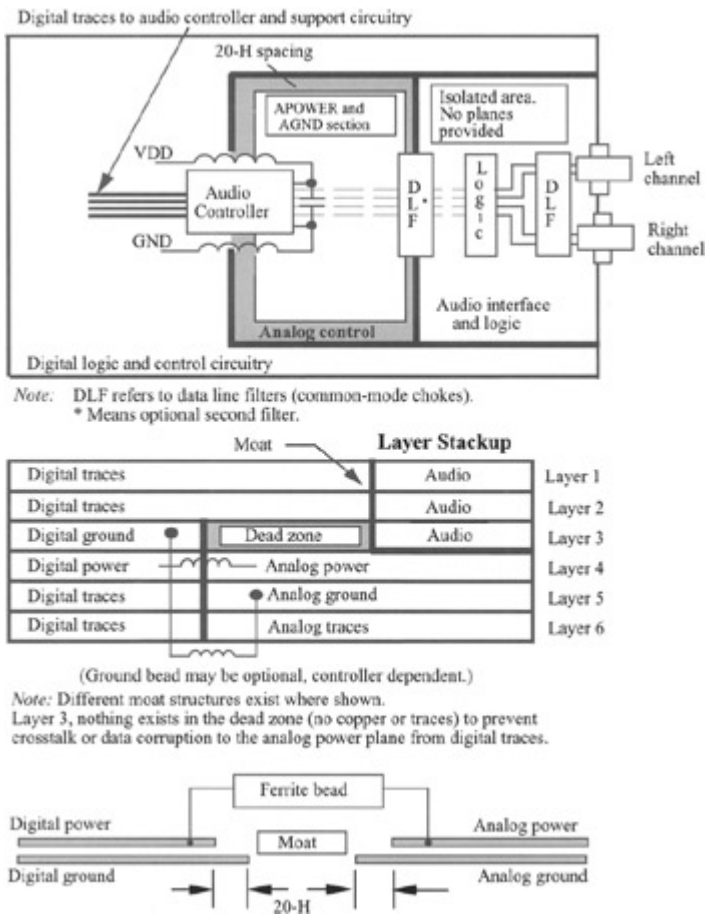

Figure 5.15: Audio circuitry layout concept.

When designing a moat structure for analog power and ground, route traces between the digital and analog section in the area immediately adjacent, or under the audio controller, using a ferrite bead between analog/digital power and ground. If a common ground plane is used for both analog and digital components, only the power plane needs to be moated (isolated). The *20-H rule* should be used only on the analog power plane (Fig. 5.15).

Depending on how the audio controller is partitioned, analog ground and digital ground may be connected together. If the controller requires a full partitioned analog ground from digital ground, a ferrite bead becomes mandatory. Sometimes only the power plane is moated. If a multilayer assembly is not provided, a trace must be used, also filtered.

All interconnect traces not associated with the audio controller must traverse through a bridge located directly under the audio controller and physically adjacent to a solid reference (image) plane. Violation of any trace over the moat, not traveling through the bridge, separating the analog to digital partition, will allow digital switching noise, white noise, and other

electrical disturbance to be injected from the digital section into the analog section. White noise is random noise that has a constant energy per unit bandwidth throughout the frequency spectrum. Power supply and system noise is usually heard as a 50/60 cycle hum and is not classified as white noise.

The audio interface must be treated differently from both the digital logic and analog control section. To prevent chassis switching noise from coupling to the audio I/O cables, ***complete isolation of the digital power and ground planes is mandatory.*** An audio cable usually consists of a two-wire pair: signal and return for each channel. If this type of two-wire cabling is used, the audio I/O interface connector must be isolated from the rest of the PCB using a moat.

Data line filters must be used to remove common-mode currents injected into the audio section from the external cable, as well as providing isolation from an ESD event or RF-induced energy onto the interconnect. In addition, a second set of data line filters between the analog section and audio interface should be provided. ***Do not incorporate a ground choke or inductor to reference "analog"*** **ground to** ***"audio"*** **ground.** A ground choke, or inductor, places inductance into the ground circuit. This inductance causes the transference of board-induced noise voltage to be passed from a noisy part of the PCB into a quiet or clean audio section. The filter circuit must be placed directly at the point of entry.

Analog traces and components must be located within the isolated analog section. This placement prevents coupling between the digital section to analog. This partitioning is illustrated by a "dead zone" on Layer 3 in Fig. 5.15. Use of the *20-H rule* may also be required in the analog section of the PCB. It is preferred that the surrounding reference planes be at ground potential rather than power in order to minimize crosstalk or digital switching noise that may exist within the planes.

If using a cable with a RF braid (similar to a shielded two-pair instrumentation cable), a bypass capacitor (typically 0.01 µF) is used to connect the braid of the audio cable directly to chassis ground. Thus, the braid, or mylar foil shield of the cable will be signal return, not RF ground or RF shield. Bypass capacitors remove high-frequency RF energy from corrupting audio quality while allowing compliance with EMI requirements. Different vendors of peripheral devices such as speakers and joysticks do not terminate the braid of the interconnect cable.

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Chapter 6: Electrostatic Discharge Protection

6.1 INTRODUCTION

Printed circuit boards must incorporate protection against electrostatic discharge (ESD) events that can enter I/O interconnects and locations that a user can physically touch. The goal is to prevent component or system failure resulting from externally induced high-voltage level impulses that may affect system operation through both radiated and conducted means.

An ESD event starts with a very slow buildup of energy (seconds or minutes) which is then stored in the capacitance of a structure (e.g., a human body, furniture, or unconnected cable). This charge is followed by a very rapid breakdown (typically within nanoseconds). With this pulse in the nanosecond range, the discharged energy can produce EMI in the frequency range of hundreds of megahertz to beyond one gigahertz. An ESD event from a human can exhibit rise times ranging from approximately 200 ps to greater than 10 ns, with peak impulse currents from a few amperes to greater than 30 A [2]. Because of its high-speed, high-frequency spectral distribution, ESD energy can damage circuits, bounce grounds, and even cause upsets through electromagnetic coupling.

A detailed discussion on waveforms, equivalent ESD circuits of humans, furniture, and other materials is beyond the scope of this text. Many excellent references are provided at the end of this chapter for those interested in both a mathematical and technical analysis of this subject.

Before providing design techniques to prevent ESD damage in PCBs, the ESD event itself must be understood. This will make the design techniques presented later in this chapter easier to understand and implement.

Humans, furniture, and simple materials such as paper or plastic generate ESD pulses. This high-energy pulse may travel through multiple coupling paths, including circuits and grounds, or may even be radiated as a transient electromagnetic field. ESD creates multiple failure modes including damage, upset, lockup, and latent failures.

In addition to current levels, ESD rise time is also important. ESD is a very fast transient. Two parameters are of great concern: peak level of current and rate of change (dI/dt). In the EMI world, rise times are equated to a frequency spectral distribution based on the Fourier transform, which relates time domain signals (edge rates) to frequency domain components, as explained by Eq. (6.1):

(6.1)
$$f = \frac{1}{\pi t_r}$$

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where f is frequency in hertz, and t_r = edge rate transition time. Given this discussion, a typical 1 ns rise time exhibits a spectrum of over 300 MHz. As a result, immunity design and layout techniques are required, similar to

those used to minimize EMI energy.

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6.2 TRIBOELECTRIC SERIES

Electrostatic discharge (ESD) is a natural phenomenon that affects materials of different potential. This difference in potential occurs as a result of accumulated electric charges. Static electricity is generated when two materials rub against each other, each with a different dielectric constant. When an excessive number of electrons accumulate, they discharge to another material with a lower concentration of electrons to balance out the charge. The effect of the discharge, resulting in electromagnetic disruption, can vary from noise and disturbance in audio or measurement equipment to complete destruction of sensitive components, including electric shock to a person who has been energized.

ESD introduced through a conductive transfer mode must be considered in terms of current flow, not voltage. It's like a burst dam—it is the water flow that does the damage, not the pressure that was behind the dam before it burst. Voltage is merely a convenient metric of the electrostatic "pressure" before the ESD event occurs [3]. ESD introduced through direct or indirect means must be viewed with respect to both electric and magnetic fields, derived from voltage and impulse current components.

A buildup of energy must result before discharge occurs. When two materials are rubbed together, with at least one being a dielectric, an accumulation of a positive charge occurs on one material, while the other material receives a negative charge. The farther apart on the triboelectric scale, the more readily the charge will accumulate. The triboelectric scale (Table 6.1) represents, at the atomic level, the charge density distribution related to polarity. This table is to be used only as a guideline and is accurate to a degree, depending on material composition. The material at the top of the table, Item 1, easily gives up electrons and therefore acquires a positive charge. The materials at the lower portion of the table, Item 36, absorb electrons, thus accumulating a negative charge.

Table 6.1: Triboelectric Series

Open table as spreadsheet

POSITIVE CHARGE	
1. Air	19. Sealing wax
2. Human skin	20. Hard rubber
3. Asbestos	21. Mylar
4. Rabbit fur	22. Epoxy glass
5. Glass	23. Nickel, copper
6. Human hair	24. Brass, silver
7. Mica	25. Gold, platinum
8. Nylon	26. Polystyrene foam
9. Wool	27. Acrylic rayon
10. Fur	28. Orlon
11. Lead	29. Polyester
12. Silk	30. Celluloid
13. Aluminum	31. Polyurethane foam

14. Paper	32. Polyethylene
15. Cotton	33. Polypropylene
16. Wood	34. PVC (vinyl)
17. Steel	35. Silicon
18. Amber	36. Teflon
	NEGATIVE CHARGE

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6.3 FAILURE MODES FROM AN ESD EVENT

Most ESD problems fall within two categories—component damage and operational disruption:

- *Component damage:* Occurs whether or not the component is installed in a circuit. A semiconductor affected by ESD fails because of junction puncture burn-through or fusing. This type of damage is permanent and easy to detect. A subtle type of damage is weakening of the component. When subjected to an ESD event, the circuit is partially damaged but still fully functional. When stressed by a power supply, high temperature, or abnormal operating conditions, the damaged component can then fail permanently. This latent effect is very difficult to identify and solve.

- *Operational disruption:* Caused by either direct or indirect injection of energy. Direct discharge occurs when ESD current finds its way to circuits through ports: power, ground, input, or output. When a sufficient amount of current is present, circuits will react. Permanent damage is possible, and operational errors may be observed. For logic circuits, state changes can occur, causing program halts and memory scramble.

The definition of direct and indirect discharge follows.

- Direct discharge is the discharge directly to the equipment under test (EUT). It may be by direct galvanic contact between source and circuit, or it may be by a discharge through air to metallic items (e.g., traces) on the PCB.

- Indirect discharge occurs to an adjacent metallic surface by electromagnetic radiation. The radiated fields couple to the circuit.

Damage to a component is determined by the device's ability to dissipate the energy of the discharge or to withstand the voltage levels involved. This concern is identified as device sensitivity to an ESD pulse. Some devices are prone to ESD damage while others may be robust. Damage can occur at any time. Most devices are susceptible to ESD damage at relatively low-voltage levels, such as 100 volts. Many disk drive components are sensitive to discharges above 10 volts. Component technology has progressed to the point where potential problems will develop under various environmental conditions, and at low levels of energy disruption.

There are four basic failure modes from ESD-related events to PCBs [1, 3]. The first three are shown in Fig. 6.1.

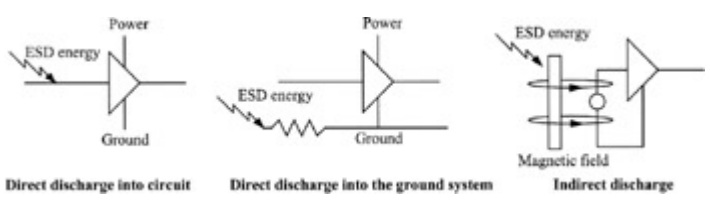

Figure 6.1: Failure modes caused by an ESD event.

1. *Upset or damage caused by ESD current flowing directly through a vulnerable circuit*. This relates to any current discharged directly into the pin of a component that causes permanent failure. This condition can occur when handling a PCB or digital component. Through this mode, direct discharge to the component from the outside environment (e.g., keyboard) can carry damaging ESD energy. Even

a small amount of series resistance or shunt capacitance will limit the ESD current, although the acceptance value is specific to each component type.

Solutions to this problem include ESD-handling requirements during installation or maintenance. Digital circuits have little ESD protection designed into the silicon wafer. For interconnects, damage typically occurs when a charge buildup is carried from the body of the installer to the connector backshell. The backshell then discharges directly to the signal pins. To prevent damage from a connector discharge, it is important to provide a filtered connector designed to dissipate ESD energy directly, or to use a connector with mating pins recessed deeply inside the housing.

2. *Upset or damage caused by ESD current flowing in the ground circuit*. This situation typically occurs in systems where chassis ground is directly connected to circuit ground. Most circuit designers assume that all circuit grounds have a low-impedance path to chassis ground. Once ESD gets injected into the circuit ground, problems will be observed anywhere within the PCB and are nearly impossible to stop. A discharge to metal results in currents traveling in unpredictable paths, often upsetting circuits but not necessarily destroying them. Current distribution does not follow intended circuit paths with fast rise-time transitions. A small amount of stray capacitance becomes a low-impedance path because wires are too inductive to pass the current. The current follows a ground path rather than a signal path.

   With a 1-ns rise time for an ESD event, ground impedance may not be low. Hence, the ground will "bounce." The usual result is an upset. Ground bounce, or level shifting of the 0V-reference, can drive CMOS circuits into latchup. Latchup is a situation where the ESD doesn't actually do the damage—it just sets things up so that the power supply can destroy the part or, at best, the circuit becomes nonfunctional without a power cycle reset.

   The ground discharge problems can be resolved by ensuring that all locations receiving the ESD energy have a low-impedance ground path to the remainder of the enclosure. A low-impedance connection must be by a direct bond or ground braid. The length of the braid cannot exceed a width to length ratio of 5:1. Width is better than length! Braid dissipates ESD energy quickly.

   If a plastic enclosure is provided, grounding to metal parts cannot be performed. For this application, one must insulate or recess all metal parts and assemblies to prevent a direct discharge. Metal assemblies need to be connected together by a 10K to 100K ohm resistor to keep peak currents from traveling between assemblies. These resistors do not affect the 0V-referencing between assemblies. If a lot of metal is located in close proximity, the resistor will not work, as capacitive coupling will dominate.

3. *Upset caused by electromagnetic field coupling (indirect discharge)*. This effect usually does not cause damage, although damage to very high-impedance components can occur. Damage is rare because only a small fraction of the ESD energy is coupled directly into the vulnerable circuit. The induced voltage is usually not enough to do more than upset the logic. This failure mode depends heavily on the rise time of the discharge (dI/dt) and circuit loop area, regardless of shielding. This effect is often called the indirect coupling mode. Electromagnetic field sources do not have to be very close to cause disruption to sensitive circuits. Tests performed to ensure ESD protection levels are identified as the air or furniture discharge model.

   The indirect discharge is produced by intense magnetic field coupling to adjacent current loops. Coupling increases with loop area. Loop areas of a PCB allow for radiated emissions to exist, in addition to permitting external magnetic fields to enter the circuit. This type of event is generally observed on products packaged in plastic enclosures, where an external discharge couples directly to internal circuits by electromagnetic means.

   The solution to preventing a discharge from upsetting circuits is to minimize loop areas on the PCB. Multilayer boards are preferred

owing to their smaller loop sizes. Loops on double-sided boards can be minimized by careful layout. Routing of cables and interconnects to the PCB must be as close to metal return paths to minimize loops that may be present. Cables routed across cable seams are optimal for reception of intense magnetic fields.

4. *Upset caused by a pre-discharged (static) electric field*. This failure mode is not as common as the other modes. This mode appears in very sensitive, high-impedance circuits.

   A pre-discharged (static) electric field is caused by stripping electrons from one object (resulting in a positive charge) and depositing these electrons on another object (resulting in a negative charge). In a conductor, charges recombine almost instantly, whereas in an insulator, the charges can remain separate. In an insulator, it may be a long time before significant charge recombination occurs and, consequently, a voltage builds up. If the voltage becomes large enough, a rapid breakdown occurs through the air or insulator, creating the familiar ESD arc or spark.

Because ESD is transient in nature, fast digital circuits are more prone to ESD upsets than slow analog or, for that matter, low-bandwidth digital device circuits. In fact, ESD rarely upsets the functionality of analog circuits. However, both analog and digital circuits are vulnerable to ESD damage from a direct discharge. Digital circuits with edge rates faster than 3 ns are particularly vulnerable because phantom ESD pulses can fool them. As a result, digital circuits are more vulnerable than older circuits with slower edge rates.

To illustrate the intensity of an ESD pulse, rise times of 500 ps or faster have been measured. With this knowledge, an ESD pulse with a rise time of 500 ps and tens of amperes of peak current translates to an equivalent slew rate of giga-amperes per second across the circuit interface.

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6.4 DESIGN TECHNIQUES FOR ESD PROTECTION

Fundamental concepts for preventing damage to a PCB from an ESD event involve reducing field coupling. All techniques listed here are used for the proper EMC design of PCBs, which helps to eliminate ESD coupling and interference but not necessarily damage components and circuits [4]:

1. Use filters to attenuate the energy at the source.
2. Use filters to attenuate energy received at the load.
3. Reduce coupling by separating components from each other.
4. Reduce coupling efficiency between source and load.
5. Reduce coupling efficiency by orienting susceptible devices perpendicular to areas susceptible to ESD corruption.
6. Install a metal shield over components and assemblies properly grounded.
7. Reduce electric field coupling by decreasing the impedance of the transmit and receive antenna.
8. Reduce magnetic field coupling by increasing the impedance of the antenna.
9. Couple signal lines to a ground structure.

Items 7 and 8 have opposite effects and are difficult to accomplish efficiently. Thus, they are not considered a viable solution or design technique.

Main areas of concern, also discussed in this section, include

1. Minimizing loop areas.
2. Keeping trace lengths as short as possible.
3. Providing ground fill or a low-impedance path for the discharge to travel to.
4. Making proper use of decoupling and bypass capacitors.
5. Isolating electronic components from the source of an ESD event.
6. Ensuring chassis ground connection is low impedance and well isolated.

The overall priorities of the design rules to be presented are to

1. Prevent charge injection into PCB circuitry, resulting in destruction or disruption.
2. Prevent problems due to fields generated by discharge currents.
3. Prevent electrostatic field problems.

Although the majority of direct ESD problems are cable related, any place where humans can come into contact with the circuit or system may cause disruption. The solution is straightforward—protect all lines, including signal, power, and ground path. The objective is to prevent ESD current

from entering the PCB with a high series impedance such as a resistor, ferrite bead, or capacitive filters. Another technique is to provide a low-impedance path to ground. The problem with a low-impedance path to ground is that we have now set up a ground bounce situation. On a multilayer board, with a ground plane, the ground impedance is usually low enough that ground bounce is not a major concern.

In cases where cable shielding is inadequate or lacking, attention to suppression of the transient energy at the module or component level is required. If the intended measurement is within an analog system, whose signals vary slowly, a low-pass filter arrangement may be provided to reject the high-frequency content of a typical ESD event. This filter eliminates the transient, allowing the desired signal to pass through. If an *LC* filter is provided, in an *L*-section topology (series inductor, parallel capacitor), the inductor will help increase the impedance of a low-impedance circuit. The capacitor will help to reduce the impedance of a high-impedance circuit.

When field coupling of a discharge occurs, with respect to an I/O cable, the noise transient coupled into the system is common-mode. This means that the coupled energy is applied to all cables or interconnects at the same time and with the same polarity. A ferrite core rejects common-mode energy when placed over the cable assembly. This ferrite core rejects common-mode noise while passing the differential-mode signal of interest. A disadvantage of using ferrite cores is the physical size of the device, along with cost.

6.4.1 Single- and Double-Sided PCBs

Single- and double-sided PCBs are extremely prone to upset or damage from ESD events, by either direct or indirect discharge. Very few design techniques are available, with the primary objective being to keep the event from reaching the PCB in the first place. The high ground impedance can easily combine with ESD to generate ground bounce in excess of many volts. A ground plane used in a multilayer board will reduce ground bounce to a few millivolts, which is an acceptable level for most logic devices.

For a single- or double-sided PCB, ground impedance is extremely high. Ground bounce becomes the primary concern. Connecting filter capacitors to ground provides no benefit. If a good ground plane, or 0V-reference, does not exist to transfer the ESD currents into, a high-impedance series element becomes mandatory for *each* signal line. Using filter capacitors will not work, because the capacitor will transfer the current into the ground circuit. The requirement is to keep high current levels out of the ground system. Figure 6.2 illustrates this situation. With a ground trace between devices, the impedance in the trace is high enough to cause the ESD current to enter the first device the current sees, in this case, device 1.

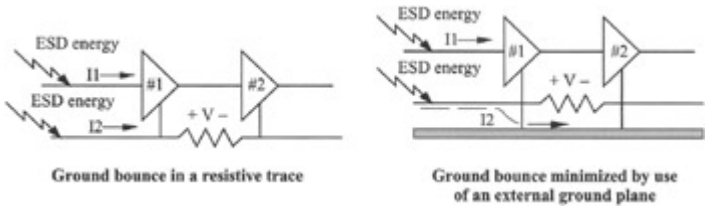

Figure 6.2: Ground bounce in single- and double-sided PCBs caused by an ESD event.

One way to minimize ESD damage is to provide an external or auxiliary ground plane directly adjacent to the PCB. This ground plane can be an inexpensive sheet of aluminum-back mylar foil or similar material. By providing a low-impedance connection to the auxiliary plane, improvements have been observed by increasing the failure of products from 2 kV, direct injected pulse, to 15 kV without damage to any components. The *ground traces* must be connected to the *ground plane* at numerous intervals. Numerous intervals prevent the ground system from bouncing, causing latchup of CMOS components or altering the reference level for both analog and digital circuits. Generally, ground connections at critical points (processors, memory, I/O interconnects, and the like) are required. The auxiliary ground plane must be located as close as physically possible to minimize the impedance of the ground connection.

Another area of concern is loop area control on single- and double-sided PCBs. This concern is by virtue of component placement and layout. An

example of an excessive loop area is shown in Fig. 6.3 for various topology layouts. This loop presents problems for both radiated emission and immunity protection.

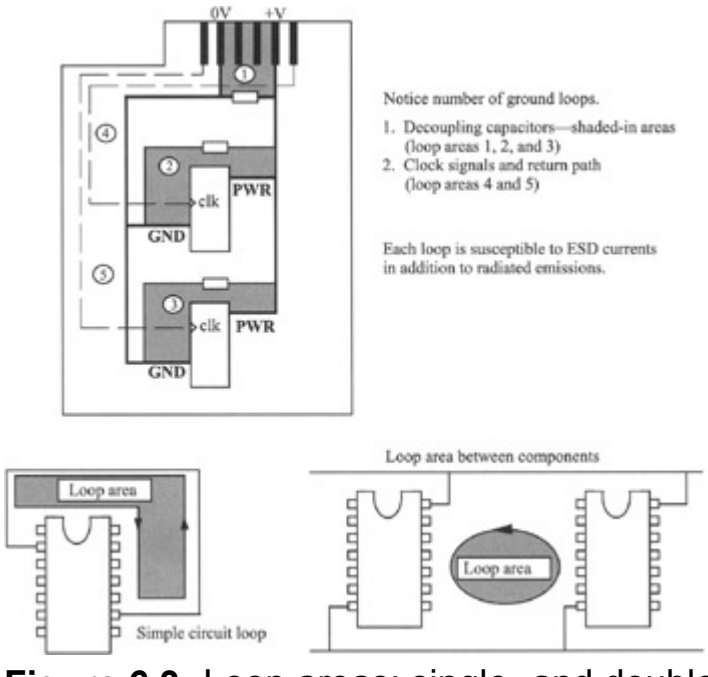

Figure 6.3: Loop areas: single- and double-side layouts.

To minimize loop areas on single- and double-sided PCBs, related to both EMI and immunity, the following are recommended (detailed in Fig. 6.4):

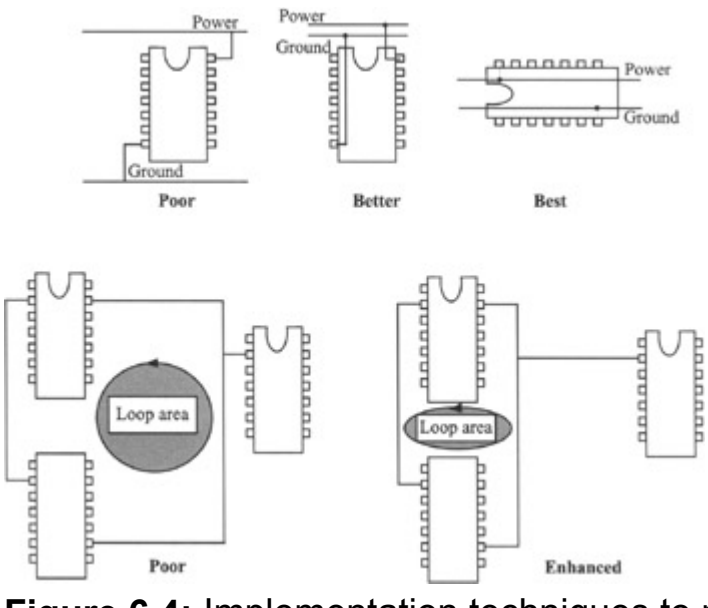

Figure 6.4: Implementation techniques to minimize loop area on single- and double-sided PCBs. (Source: Boxleitner, W. Electrostatic Discharge and Electronic Equipment. 1989. Reprinted by permission—IEEE Press.)

1. Route power and ground traces adjacent to each other with minimal distance spacing between the two.

2. If multiple power and ground traces are required, connect them together in a grid fashion. Each grid provides a smaller loop area than if no grid existed. This small loop area results in lower induced currents and magnetic field coupling.

3. Route parallel signal traces close together to minimize the RF return current loop area.

4. Route signal traces as close as possible to a ground trace. Use of a ground grid helps implement this requirement.

5. Use high-frequency bypass capacitors between power and ground containing a low-impedance value at ESD frequencies. ESD is generally considered approximately a 300-MHz event. A capacitor that is self-resonant at 300 MHz means the value would be in the mid-picofarad range. These capacitors generally cannot handle large amounts of transient currents. Lead inductance may also make these capacitors ineffective for use in bypassing ESD energy.

6.4.2 Multilayer PCBs

Design techniques for ESD protection that can be implemented on a PCB for high-level pulse suppression include the following, divided into three

sections: components, circuit layout, and system level.

Components to Prevent ESD from Entering the PCB. Components are commonly used to prevent coupling an ESD event to circuits susceptible to being upset. These transient suppression devices consist of discrete components or filter modules. When filters are provided, the location of the device is the critical aspect of implementation. Filters must be as close to the energy source as possible. Filters and transient suppressors can be thought of as a barrier between zones, designed to reduce or eliminate unwanted voltages and currents that might otherwise travel between zones.

If energy is captured prior to entering the system, maximum benefits occur. One benefit is preventing re-radiation of the pulse to the inside of the product. All filters require a high-quality RF impedance path to ground. These filters must be chosen for a particular application and may consist of various topologies. For enclosure and board-level-based filters, bonding to the chassis is required. This low-impedance path is accomplished by use of short, wide traces from the mounting pin of the bypass element to a conductive standoff, mounted directly to the device chassis.

When using a filter element, one design technique to maximize effectiveness is to provide a separate I/O interface module mounted directly at the cable entry location. This I/O interface may be multilayer with ground plane(s) to allow connection to the filter components. This I/O interface must incorporate two items. First, the filter must be located directly at the input without any exposed wires. Second, efforts can be made for an enhanced filter board without having to provide design constraints on the primary PCB.

Filter and transient suppression components include the following:

1. *Spark gaps*. Spark gaps are sharply pointed triangles created within the copper of microstrip layers aimed at each other. This design technique is totally "impractical" for ESD protection. The topic of spark gaps is examined for historical reasons.

   The pointed tips are separated by a maximum of 0.010 in. (0.25 mm) and a minimum of 0.006 in. (0.15 mm). One triangle is connected to the ground plane, while the other triangle is part of the signal trace. These triangle spark gaps must be placed only on the outer layer of the PCB, with no soldermask. A soldermask provides a dielectric insulator (barrier) that prevents ESD energy from jumping between the two triangles. The only signals, or I/O connections exempt from use of spark gaps, are those mandated by regulatory safety agencies to pass dielectric withstand tests (hipotting). Implementation of a spark gap is shown in Fig. 6.5. Hermetically sealed spark gaps, available as a component, are generally too slow in responding to an ESD event. Thus, they provide only minimal effectiveness for the intended application and are more suited to transient surge protection in power supplies connected to an AC mains source.

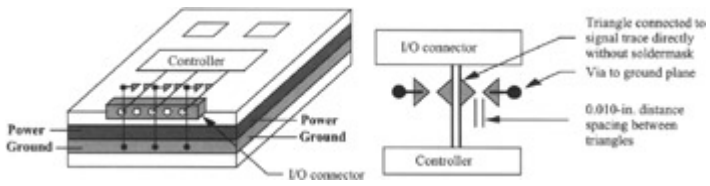

Figure 6.5: Spark-gap implementation.

   Air-type spark gaps, if used in an area that is subject to frequent ESD events, will eventually break down and create carbon tracking when an arc occurs between the two triangle points. Carbon is a conductive material that could eventually short out the spark gap. The net result is that the signal trace can be permanently shorted to ground. As a result of carbon tracking, use of air-type spark gaps is not recommended in open-air installations where ESD events frequently occur. However, hermetically sealed spark-gap components are usually stable over time.

2. *High-voltage capacitors*. For ESD events, high-voltage disc-ceramic capacitors are required to shunt energy to chassis ground, not system ground. These capacitors should be rated at 1500V (1kV) minimum. Lower-voltage capacitors may be permanently damaged upon the first occurrence of an ESD event. This capacitor must be located

immediately adjacent to the I/O connector with as small as possible lead inductance. In regards to electrical fast transients, capacitors rated at 50V to 100V are usually sufficient. These capacitors will not break down from a short transient since they will not be able to respond to the fast incident event. Because the transient event is short, the voltage buildup is low and the capacitor will not break down.

3. *Avalanche Diodes (Tranzorbs*[1]). Avalanche diodes are semiconductor devices specifically designed for transient voltage suppression applications. They have the advantages of a stable and fast time constant to avalanche, or trigger, along with a stable clamping level after they turn on. These diodes must be fast enough to react to the ESD event, and they are designed to dissipate a lot of energy in a short time period. For optimal performance, the leads must be kept short. A few millimeters of lead length will degrade the performance of this protective device. High-frequency capacitors may be used in parallel to slow down the ESD pulse, thereby giving the transorbs sufficient time to clamp. Avalance diodes are available in I/O connectors for protection against an ESD event. These diodes are connected to chassis ground within, not to circuit ground or 0V reference.

4. *LC filters*. A *LC* filter is a combination of inductors and capacitors. These components prevent high-frequency ESD energy from entering the system. The inductance presents a high-impedance source to the pulse, thus attenuating energy attempting to enter the system. The capacitor shunts high-frequency ESD energy to chassis ground. An additional benefit of this circuit combination is preventing radiated EMI from being projected onto an external cable interconnect. The filter minimizes RF energy by rounding or rolling off the edge transitions of the data signals. Rolling a signal transition may, however, compromise signal integrity.

5. *Non-ESD sensitive components*, such as diode-protected CMOS or TTL. These can be used in circuits susceptible to ESD disruption. Ensure that these components have clamping diodes provided internal to the silicon wafer.

6. *Bypass capacitors with a high self-resonant frequency between power and ground*. These bypass capacitors must have equivalent series inductance (ESL) and equivalent series resistance (ESR) that are as low as possible. Frequent use of bypass capacitors reduces the loop area between the power and ground planes for low frequency, high-level pulses. For higher-frequency ESD events, standard capacitor dielectrics may become less effective owing to the capacitor's internal lead and interconnect trace inductance between the component and ground stitch connection. In addition, use of series resistors for protection of CMOS circuits is possible. These components could easily tolerate 1-kΩ series resistance in their input, limiting the ESD current entering the device.

7. *Ferrite material, beads, and filters*. These provide excellent attenuation of ESD currents, in addition to enhancing suppression of radiated emissions. Hence, two features with the use of one device are obtained when properly incorporated—emissions and immunity.

Circuit Layout

1. Use a multilayer stackup. Multilayer PCBs are superior to single- and double-sided assemblies because a stable ground layer is available. ESD must never be allowed onto the surface of a double-sided assembly. Once ESD enters a double-sided board, it becomes practically impossible to cope with the ESD event. If a double-sided PCB must be used, provide a separate ground layer, shield, or fill on the top and bottom of the board. This allows for termination of filter elements, if provided, and permits the ESD event to find a lower impedance path to ground, away from components.

   Use of multilayer PCBs provides 10 to 100 times improvement over two-layer boards for protection against electromagnetic fields from an indirect ESD event. Locate the first ground plane as close to the signal routing plane as possible. This placement allows ESD to be coupled to a lower impedance reference, thus minimizing ESD energy from

reaching signal traces.

2. Filter critical circuits and lines. It is impossible to ascertain which traces will become susceptible to an ESD event. If this situation exists, every pin on every device requires filtering, a task that is expensive, parts wise, preventing ESD energy from being routed toward the PCB circuitry.
   - ESD contains a very fast, high current pulse but little energy; hence, filter elements need not be large in size. Do not use a small value for the bypass capacitors. These capacitors charge up quickly to unacceptable high-voltage levels. If one cannot filter high-speed circuits, use transient suppression devices. Metal oxide varistors (MOVs) and arc suppression components react too slowly to protect circuits from a high-speed ESD event.
   - Analog lines generally do not need ESD filters; however, a filter may be required for EMI purposes. Outputs of analog devices are less susceptible to indirect ESD and often do not need protection. Input lines of digital components are very vulnerable and should always be filtered.
   - Terminating filters to circuit ground is risky. A multilayer PCB may be able to absorb ESD currents without upsetting circuits. If at all possible, terminate the filter to a shield boundary instead.
   - Apply bypass capacitors to all components, especially microprocessors and other large-sized components. Guarantee that bypass capacitors are applied to high-impedance feedback circuits.

3. Keep a low ground impedance connection between multiple PCBs and interconnects. When one PCB communicates to another PCB through an interconnect, ensure that there are sufficient ground pins between the two. This requirement is mandatory for both EMI and ESD compliance.

4. Minimize loop areas. Identify areas where loop currents can exist. This includes the distance spacing between components, I/O connectors, and component/power planes. Keep in mind that loop areas include both signal (RF return path) and power distribution.

5. Tightly control coupling between power and ground. This is accomplished by keeping the power and ground traces as close together as possible. For multilayer PCBs, the power and ground planes must be physically adjacent to each other. Tight coupling is also achieved using high self-resonant frequency decoupling capacitors between power and ground. Current injection problems from a high-level pulse are also reduced using this configuration.

6. Fill in both the top and bottom layers of the PCB with as much copper at ground potential (ground fill) as possible. This localized fill minimizes ESD effects by providing a low-impedance path to chassis or system ground. A large metal plane, or copper fill, has a lower impedance value compared to a ground trace. This low-impedance ground fill conducts a high-energy pulse to ground, rather than allowing the energy to corrupt or enter signal lines or components. One disadvantage of using fill areas at ground potential is that an ESD pulse could be discharged into the ground system, causing potential damage to components through ground bounce. Ground bounce can cause devices to become nonfunctional, along with injecting system glitches into the operation of the device. If ground fill is provided on the outer layers of the PCB, connect the fill to the ground plane or chassis ground at frequent interval spacing not signal return ground.

7. Implement moating and isolation between ESD-sensitive components from other functional areas. Moating and isolation are discussed in Chapter 5. Isolation prevents ESD from being transmitted or coupled from one functional section to another.

8. When a multilayer PCB is provided, guarantee that the ground plane, internal to the PCB, surrounds every plated through-hole. This ground plane minimizes the creation of loop areas between circuits and traces internal to the PCB.

9. Physically connect transient protection devices to chassis ground, not

circuit or system ground. ESD events contain large amounts of current. Placing high current levels on circuit or system ground planes can cause serious ground bounce and possible component failure.

10. Keep routed trace lengths as short as possible. Traces act as an antenna for both radiated emissions and susceptibility concerns, depending on routed length. This routed length is susceptible at various wavelengths and harmonics of a particular frequency. A trace that is routed microstrip will always be susceptible to the reception of radiated ESD energy. It becomes important to group components with similar functions as close as possible in areas susceptible to ESD disruption.

11. Keep signal lines as close as possible to ground lines, ground planes, and circuits. This is illustrated in Fig. 6.6 when single- and double-sided boards are used. Do not route critical signals near the edge of the PCB.

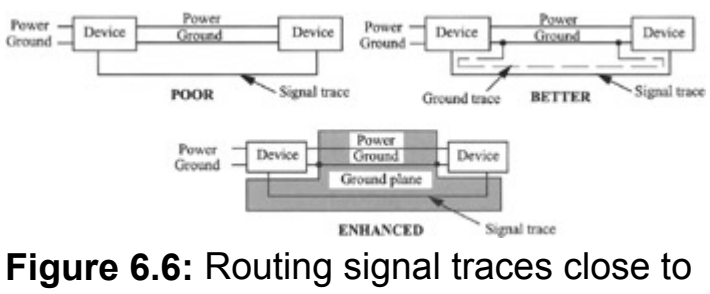

Figure 6.6: Routing signal traces close to ground.

System-Level Protection

1. Provide a complete shield around components and circuits susceptible to radiated ESD corruption. Bond the shield to chassis ground at multiple points, providing a low-impedance path for the ESD currents absorbed by the shield. If shielding is impractical, consider effective insulation. This insulation would work just as effectively for "direct discharge," not for radiated coupling of ESD.

2. Route internal cables away from slots and openings. These openings can couple radiated energy into cables or interconnects, which then transfer this energy to circuits through conduction.

3. Protect all I/O cable entries with suppressors: resistors, *RC* network, *LC* filter, capacitors to ground, ferrite beads, diodes, transorbs, or similar components. Install these suppression devices immediately adjacent to the I/O connector, with components connected directly to chassis ground.

4. Make all chassis ground connections low impedance. Locate these ground connections at positions where they will conduct ESD impulse energy away from sensitive circuits rather than through them. A low-impedance path to chassis ground will divert ESD energy. Provide a chassis ground connection with a width-to-length ratio of 5:1 or less (width five times greater than length). Keep the ground trace as short as possible. This 5:1 ratio is the maximum recommended ratio. A 3:1 ratio will generally suffice.

5. When membrane keypads for user control are provided, recess the conductive layer of the membrane to eliminate direct discharge to digital circuits. This is applicable primarily if the surface of the enclosure is nonconductive. Benefits will result even if the rest of the plastic cover is conductive.

6. Terminate conductive membrane layers directly to the enclosure shield and around the entire perimeter, even when a relatively low-conductivity material is provided.

7. Use metal housings for connector backshells. An ESD event to a connector backshell can cause serious damage, as capacitive coupling of the energy will occur to the internal wires or to circuits internal to the system. To ensure that the ESD event does not enter the connector housing through apertures in the housing, bond the cable shield to the mating backshell in a 360° fashion with a secure connection between shield and housing.

8. Avoid pigtails. Pigtails present problems for both EMI and ESD. In

addition to being a radiator of RF energy, ESD sees a loop antenna, which by virtue of typical dimensions is tuned to a particular frequency, generally the same one as the ESD event. The frequency of an ESD pulse is approximately 300 MHz (1-ns edge transition). Pigtail termination is not adequate, unless the pigtail is very short and as fat (wide) as possible. Keep the pigtail, if used, far away from signal or I/O cables. Do not terminate the shield of the enclosure directly to the PCB's ground structure—use chassis ground.

[1]Tranzorb is a trademark of General Semiconductor.

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Chapter 6 - Electrostatic Discharge Protection

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6.5 GUARD BAND IMPLEMENTATION

Guard bands are different from guard traces (discussed in Chapter 4). Guard bands are intended to minimize ESD risk to the PCB when they are handled by the edges or when they are used within a plastic enclosure. Upon handling, the board may acquire a static charge. This charge will be transferred to traces or components on the board through two coupling mechanisms, radiated or conducted. When a discharge occurs to the guard band, systemwide failure may occur.

To prevent radiated or conductive coupling into components from an ESD event, not related to external I/O cables and connectors, a 1/8 in. (3.2 mm) guard band can be placed around all edges of the PCB, both component (top layer) and circuit (bottom layer) side. The guard band should be a minimum of 0.020 in. (0.50 cm) away from components or traces. This distance separation guarantees that a voltage breakdown between the guard band and circuit is sufficient to prevent arcing of ESD current between the two. Implementation of a guard band is shown in Fig. 6.7.

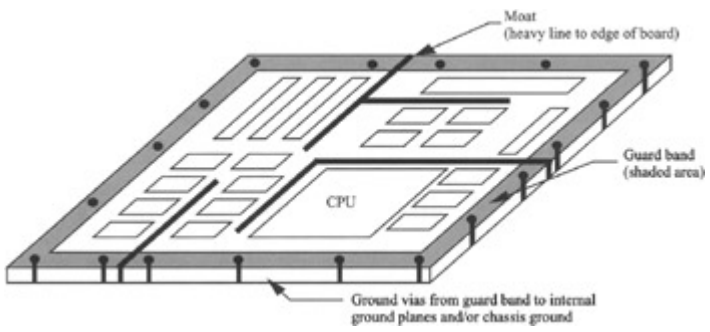

Figure 6.7: ESD guard band implementation.

The topside band is connected to the bottom-side band by vias every 1/2 in. (1.3 cm) around the entire periphery. Vias ensure that the bands are securely bonded to each other. A solid bond connection allows for a maximum amount of ESD energy to travel between the two bands, using the lowest impedance path available. When a guard band is provided, soldermask or conformal coating must not be provided to the band. Use of soldermask or conformal coating provides a dielectric barrier between the energy source and guard band. Depending on the dielectric constant and thickness of the coating, ESD energy may find an alternate, lower impedance path to ground, which is what we do not want. This alternate, lower impedance path to ground could develop as a radiated or conducted field, causing harmful results to components and devices or to the entire system.

Now comes the question—do we, or do we not, connect the guard band to the ground planes, if a ground plane is provided?

1. *Connection of the guard band to the ground plane*. The band is connected to the ground planes if the PCB is installed in a metal enclosure using a multipoint ground connection to the metal chassis. The metal chassis must also be connected to the third-wire ground, commonly identified as Protector Earth (PE). The ground between the PCB and chassis must be of a low-impedance type, securely bonded. The purpose of connecting the guard band to the ground plane for this application is to allow the ESD energy to have a very low-impedance path to a large metal enclosure at ground potential. If a low-impedance bond is provided, the ground plane should not bounce, synchronous with the ESD event. Bouncing of the ground

plane can cause destruction or malfunction of digital components. The ESD energy is essentially drained out of the system.

2. *No connection of the guard band to the ground plane*. If the PCB is packaged in a plastic enclosure or connected to a single-point chassis ground at the power supply input, connecting the guard band to ground is *not* recommended, for the following reasons:
   - If the guard band is connected to the ground plane, the plane can bounce with significant magnitudes of energy, causing permanent damage to components. The energy has nowhere to go.
   - If the PCB is single-point grounded at the power-input connector, all of the ESD current will flow in a straight-line path from the point of entry on the guard band directly to the low-impedance ground point. The energy flow will be significant, destroying almost everything in its path.
   - To prevent ESD from entering the PCB, the plastic enclosure must be designed to prevent unwanted energy from penetration. Penetration can occur almost anywhere—a user interface (keys on a keyboard), switches, knobs, enclosure mating flanges, and the like.

The guard band should not be incorporated as a complete circle (surrounding the board 100% on all four sides) because a serious problem can develop. This problem deals with the physical geometry of the band. The guard band, as a complete circle, will appear to the environment as a magnetic field loop antenna. Presence of this loop antenna allows for both radiated emissions and immunity problems to exist at a particular frequency, along with their harmonics and corresponding wavelengths throughout the spectrum. If the circle is broken into several subsections, enhanced performance is observed. Enhancement occurs because the air gap between loop segments is typically 0.020 in. (0.50 mm). The width of a typical finger, hand, or other handling device is magnitudes greater than the air gap. No matter what, any energy that is located within a body will automatically touch both sides of the air gap, thus achieving the desired goal.

If a moat is used on the PCB traversing to the edge of the board, the guard band must be broken at the partition break. This break in the guard band will not degrade EMI or ESD performance (Fig. 6.7).

If the distance spacing between the break in the guard band is less than 0.020 in. (0.5 mm), parasitic capacitance can exist between the two band segments. This parasitic capacitance is capable of allowing RF energy to bridge across the gap, causing potential susceptibility problems related to both EMI and ESD, with the existence of a loop antenna.

Chapter 6 - Electrostatic Discharge Protection

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Chapter 7: Backplanes, Ribbon Cables, and Daughter Cards

OVERVIEW

This chapter provides an overview of PCB layout techniques for backplanes, ribbon cable assemblies, and daughter cards. Among the concerns that arise when designing interconnects are impedance of the trace routes, purity of the power distribution system, construction of the assembly, trace termination, signal routing topology, crosstalk, and trace length. All design rules and techniques applicable to PCB layout presented in earlier chapters also apply to backplanes, ribbon cables, daughter cards, and motherboards with adapter slots.

The word "interconnect" is used throughout this chapter to denote backplanes, ribbon cable assemblies, and daughter cards. In other words, this chapter deals with plugging one electrical assembly or interface into another, regardless of implementation technique or verbiage.

It is a good practice, whenever possible, to design the motherboard before the daughter boards. This applies only if the entire system is under "new design" status. It does not apply when modifying an older system.

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7.1 BASICS

Before designing an interconnect, one must first determine the connector pin assignment. Assigning connector pinout at this stage helps prevent crosstalk, maintains impedance, reduces radiated emissions, and provides for enhanced signal quality performance while maintaining proper ground loop control for EMI compliance. An interconnect is essentially the *freeway* of signal flow between interface circuits and adapter cards or backplanes. As such, care must be taken to ensure optimal performance at all times.

Impedance matching between two PCB assemblies is a primary requirement for high-technology products. Generally, signal trace lengths are longer in a ribbon cable or backplane than equivalent trace routing on plug-in adapter cards. This is because a signal is generated on a card, and sent through two connectors (plug and receptacle), both of which may have different impedances. The signal then travels down a trace in the backplane, and then goes through another set of connectors to a destination point. The destination has to receive this transmitted signal and transfer it to its appropriate receiver (load). A long transmission line may exist for this signal trace route.

Because backplanes have large via holes, where the trace enters at the connector location, a decrease in impedance is observed every time a PCB is inserted. Typically, trace impedance (Z_o) is 45 to 70 Ω. Large-size vias in the backplane can drop overall trace impedance significantly. With lower trace impedance, more current is required, according to Ohm's law. An increase in drive current allows additional RF energy to exist. This RF current can then couple to other circuits, subsystems, or free space. The greater the number of board plugs into a backplane, the lower the impedance. The impedance change can easily approach 30 to 40 ohms.

Microstrip or stripline impedance-controlled connectors, though more expensive than traditional connectors, reduce or eliminate any impedance mismatch that may occur between adapter cards, backplane, cable assembly, or motherboard. Both connector styles contain a very large pin count. The net result is higher performance of the interface and optimal signal quality for reliable operation. With proper layout and design techniques presented in earlier chapters, higher quality data and clock signal traces are possible within backplanes and daughter card designs.

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7.2 CONNECTOR PINOUT ASSIGNMENT

The major source of RF energy developed in a system is generated from the physical connection between a backplane and motherboard or between a motherboard and daughter card. An imbalance in differential-mode wave propagation is one method of developing common-mode energy, which then causes EMI concerns. This interconnect is performed by either cables or connectors. Differential-mode RF current is developed by many sources. EMC compliance is generally neglected when backplanes, ribbon cables, daughter cards, and interconnect pinout assignment are designed or specified.

Backplanes, or poorly designed interconnect assemblies, usually consist of multiple signal traces in parallel, including clock signals, sharing a single common ground-return pin or lead. Many design engineers will allocate only one ground pin in a multi-pin connector, assuming one ground pin is adequate for the connector. In reality, one ground pin is required for each signal pin for optimal performance, which will double the amount of I/O connector pins required. If designing a proprietary interconnect structure, it is simple to specify an optimal pinout for performance reasons before freezing the design.

When ground pins are assigned throughout the entire length of the connector, ground loop areas must be minimized to prevent high-amplitude levels of RF currents from being coupled to other components or subsystems. Loop control on the PCB can be maintained using a multilayer stackup, with both 0V-reference and alternating ground pins between clock and signal lines on the interface connector. An example is shown in Fig. 7.1.

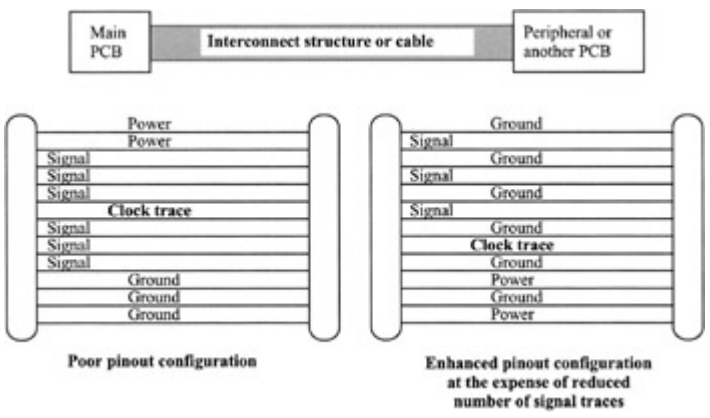

Figure 7.1: Recommended layout of ground return pins for interconnects.

When designing interconnects, consideration must be given to all clock and periodic signal traces. ***A clock trace must always have an adjacent RF return path on all sides of the connector or interface.*** This is shown in Fig. 7.1 under enhanced pinout configuration.

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7.3 AC CHASSIS PLANES

Some applications require use of an AC chassis plane in addition to 0V-reference planes. This AC chassis plane has no direct connection to other reference planes, except through bypass capacitors (usually 0.1 µF). The AC chassis plane must, however, be physically located directly next to a 0V-reference plane, providing very tight capacitive coupling between the two, thus minimizing use of discrete capacitors. At high frequencies, these planes are effectively tied together because of interplanar capacitance between the two. The AC plane always connects to a metal chassis along a continuous axis. At high frequencies, we have shorted the digital 0V-reference plane to chassis. This coupling reduces the amount of digital ground noise at that point, sending it into the chassis, also reducing signal noise transmitted by the source driver to the outside world.

When using an AC chassis plane, the digital logic return plane must be electrically isolated at low frequencies from chassis potential. This isolation may also be desirable for safety or other reasons. If isolation is not important, the AC chassis and 0V-reference planes may be shorted together.

Bypass capacitors, if provided between 0V-reference and chassis, shunt RF currents generated in the internal reference planes without degrading functional performance. One item to note is that ordinary capacitors will not function as an optimal short between chassis and 0V-reference because there is too much lead inductance in the capacitor. Only a large, wide, parallel surface area between the chassis plane and digital 0V-reference plane will have a low enough inductance to effectively short the two planes together.

When a chassis plane is provided on the outer layer of a backplane assembly, another chassis plane should also be provided on the opposite side of the stackup. This balance in board stackup assignment is required during the manufacturing cycle to prevent warping.

Use of a chassis plane is generally required in high-speed systems with edge transition rates faster than 1 ns. The 0V-reference planes must still be connected together, with as many ground vias as possible throughout the entire physical length of the backplane.

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7.4 BACKPLANE CONSTRUCTION

There are basic concerns related to daughter cards, ribbon cables, interconnects, and plug-in modules when defining overall construction and configuration. These concerns are in addition to the information presented throughout this book. Consideration must be made to determine if routing on the outer layers of the assembly (microstrip) or inner layers (stripline) is to be performed. Generally, a plug-in module is positioned at a 90°, or orthogonal angle to the main board (e.g., adapter boards for personal computers) or card cage assemblies where the modules are plugged into a backplane.

Five areas considered in this section are

1. Purity of the power distribution system from noise-induced voltage and high-frequency RF currents injected into the planes.
2. Signal quality of the bus that contains parallel traces (crosstalk concern).
3. Impedance control and capacitive loading for each trace route.
4. Interboard coupling of RF currents (radiated coupling between two boards).
5. Field transfer coupling of daughter cards to card cage (daughter card corrupting its plug-in module).

POWER PLANE PURITY. Switching noise from the power supply, radiated or conductive coupling of RF currents, voltage drop (IR), and ground bounce affects the purity of the voltage distribution system provided for all components and adapter cards.

Contamination of the power and ground plane is possible, which affects the performance of sensitive components, especially analog or PLL circuits. This contamination may be caused by switching noise from a power supply, externally induced RF fields, ESD, electrical overstress (EOS) events, I/O cables and interconnects, peripherals with motors, and magnetic components injecting inductive switching noise into the power distribution system (disk drives). Contamination of low-voltage sensitive circuits may also cause functional degradation to occur.

Voltage drop may occur when multiple boards are inserted into a backplane slot, with one board consuming more power than another lower-power-consuming board inserted at the opposite end of the assembly. This IR drop between boards may affect functionality and signal integrity.

Ground bounce developed internal to digital components is the largest contributor to corrupting signal integrity. Ground bounce is best observed when many large power consuming circuits switch all logic pins simultaneously under maximum capacitive load. Decoupling capacitors are provided to remove high-frequency RF currents injected into the power distribution network during a switching event. Bulk capacitors minimize *IR* (voltage) drop, maintaining proper voltage reference throughout the assembly. Consideration must also be given to eliminating ground bounce and board-induced noise voltage beyond what discrete capacitors and power and ground plants can provide. Extensive use of both bulk and decoupling capacitors must be provided for each I/O connector. This dual application of bulk and decoupling removes RF energy, or component-

induced noise voltage, maintaining signal purity in the system in addition to discrete capacitors placed on individual boards.

SIGNAL QUALITY OF PARALLEL TRACES. A concern for signal quality in a backplane lies in the large number of traces running in parallel along the length of a backplane. The items of greatest concern are crosstalk and ground slots, both discussed later in this chapter. Trace termination must also occur if the routed length of the trace is electrically long (defined in Chapter 4).

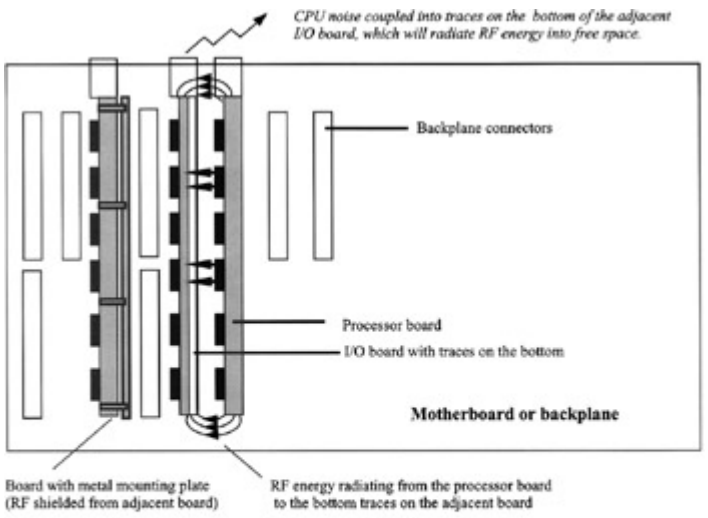
When routing parallel traces, crosstalk can become a major issue. Crosstalk is usually overlooked during layout. It is generally impossible to route traces on adjacent stripline planes using *both* horizontal and vertical trace routes on the same layer. A backplane, or ribbon cable, often has only one axis routing of traces, either horizontal or vertical. Interplane coupling from two stripline planes placed physically adjacent to each other may corrupt signal integrity on the adjacent routing plane through the process identified as crosstalk. If this situation occurs, the recommendation for large bus systems is to route each and every routing plane between two solid reference planes (voltage or ground potential). *Never route two signal planes adjacent to each other in extremely high-speed, high-technology multilayer backplanes*.

IMPEDANCE CONTROL AND CAPACITIVE LOADING. When multiple boards are inserted into a backplane, the characteristic impedance of the backplane will change owing to the capacitive loading presented by each board. In many situations, the actual impedance of the backplane can decrease to one third the desired value. Signal quality concerns and impedance control for trace termination can be seriously degraded.

When designing a backplane, an impedance study must be performed on the load characteristics and the PCB traces must be matched to this impedance value. For example, the specification for a transmission line is 100 ohms; however, a fully loaded bus may be in reality 30 ohms, after taking into consideration the total number of boards provided in the assembly. The more boards provided within an assembly, the lower the total impedance of the backplane.

If the PCB is able to operate over a wide range of impedance (i.e., 30 to 70 ohms), the value in the middle of the range should be selected (e.g., 50 ohms). Choosing a nominal impedance value for trace termination will minimize reflections in a fully loaded or no-loaded bus—the best of both environments.

INTERBOARD COUPLING OF RF CURRENTS. For multiple board configurations, consideration must be made on an individual basis, without concern as to where this board is located within the assembly or adjacent to another board containing high-threat signals. An example (Fig. 7.2) shows a high-speed processor board plugged into a backplane assembly. The processor and all digital logic components are located on the top layer. For the adjacent PCB located on the left side of the processor, signal traces are provided on the bottom layer, located directly next to the processor's components and heatsink. For this placement configuration, there exist a separation distance between boards, such as 0.100 in. (100 mils) or 0.25 in. (0.64 cm), which is extremely close physically. It is observed that RF currents from the processor will radiate into the traces that are routed on the bottom of the adjacent board, causing problems related to signal integrity and EMI due to contamination of logic circuitry. If the I/O board was relocated to a different card slot (i.e., the backside of the processor board), less RF energy would exist between the two. The solid planes internal to the processor assembly will act as a shield partition for RF currents, reducing disruption to the adjacent PCB on the back side.


CPU noise coupled into traces on the bottom of the adjacent I/O board, which will radiate RF energy into free space.
Backplane connectors
Processor board
I/O board with traces on the bottom
Motherboard or backplane
Board with metal mounting plate (RF shielded from adjacent board)
RF energy radiating from the processor board to the bottom traces on the adjacent board

Radiated coupling between boards in a backplane assembly. The I/O board is susceptible to RF corruption. High-threat traces (clocks and I/O) cannot be routed on bottom layer of the I/O board if a multilayer stackup is used.

If the I/O board is placed on left side of CPU, radiated coupling could occur from components and signal signal traces located on top side of the CPU into the bottom layer of the I/O board.

To minimize interboard coupling, make the bottom layer of I/O board a solid ground plane without trace trace routing. If not possible to have a solid plane, a metal shield partition plate may be used.

If the I/O board was located on right side of CPU, radiated coupling would not be observed, and EMI compliance may be assured, along with minimizing crosstalk disruption between boards.

Figure 7.2: Interboard radiated coupling.

With this situation, it is important to note that high-threat (clock or I/O) traces must be routed stripline when multilayer boards are used in a backplane assembly. The same concern exists for adapter cards. If design engineers forget about interboard coupling, EMI problems may be difficult, if not impossible, to locate and fix. A layout technique is to design "all" adapter boards with the bottom layer as a ground plane or at 0V-reference without segmentation from traces or split planes.

For those applications where a solid ground plane is not possible on the bottom layer of a board and coupling of RF energy occurs from an adjacent board, use of a metal shield partition may be required. This partition prevents interboard coupling. It is imperative that this shield partition be securely fastened to the PCB in as many locations as possible, which minimizes the physical dimension of a loop antenna that may exist between circuits and functional subsections on that particular board.

FIELD TRANSFER COUPLING OF DAUGHTER CARDS TO CARD CAGE. This situation is similar to interboard coupling of RF currents except that the RF fields generated from a PCB (components, ground loops, interconnect cables, and the like) can couple to the chassis, card cage, or interconnect assembly. Consequently, RF eddy currents will be present in the chassis and will circulate inside the unit, creating a field distribution. This field will couple to other circuits, subsystems, interconnect cables, peripherals, and so on. One of the most significant ramifications of this internal field distribution is to develop a common-mode potential between the backplane and card cage. This potential will exhibit the spectral energy signature not only of the backplane, but the daughter card as well. In addition, this field will be observed during radiated tests as an electric field at a distance greater than $\lambda/4$ at the frequency of concern. Proper implementation of suppression techniques on a PCB, as well as proper referencing of the backplane to the card cage to short out the distributively derived potentials, will minimize field transfer coupling between PCBs to the backplane and backplane to card cage.

Proper referencing of the backplane to the card cage takes the form of establishing a very low-impedance RF reference between the backplane and card cage. This reference method is mandatory to short out eddy currents developed at and by the daughter cards. These currents are coupled to the card cage assembly through a distributive transfer impedance, often in the low tens of ohms. This transfer impedance will allow RF energy to attempt to *close the loop* by coupling to the backplane. If the common-mode reference impedance between the backplane and card cage is not significantly lower than the distributive "driving source" (of the eddy currents), an RF voltage potential will be developed between the backplane and the card cage. This voltage will have the spectral energy signature not only of the backplane, but of all daughter cards as well. This voltage will cause any conductors that are connected to the backplane to radiate the spectral profile of the entire assembly—even DC wire. The spectral voltage developed by this mechanism will even contribute to interboard coupling using the backplane to card cage relationship as an intermediary.

Simply put, the common-mode spectral potential between the backplane and card cage must be shorted out. This may take the form of frequently connecting the backplane's 0V-reference plane to the card cage (chassis) at regular intervals around the perimeter of the assembly. Alternatively, a chassis plane can be used, positioned immediately adjacent to a ground plane. This chassis plane also serves as a "Faraday partition" within the backplane assembly. The location of a chassis plane on the outer layers must be designed such that it is *never* used as a return reference for signal traces or as an RF return path. Generally, to be reasonably effective, the RF transfer impedance between the logic ground plane and the chassis plane must be equal to, or less than, 1-Ω, thereby shorting out common-mode potential between the daughter card and backplane. This transfer impedance occurs through capacitive coupling between the two planes. For this application to work, the outer two layers must be at chassis potential, with the next two layers inward at ground potential.

7.4.1 Number of Layers

The backplane, or adapter board, must be constructed with a minimum of four layers—two routing and two potential planes (voltage and ground). Designing a backplane with less than four layers is not recommended. In a four-layer (or more) stackup, the outside layers are generally used as signal routes and the inside layers for voltage and ground, respectively.

The reader is cautioned that the best EMI and system performance will be gained when signal impedances on the routing layers are well controlled and preferably referenced to the ground planes rather than voltage planes. The intrinsic parallel-plane power impedance distribution established must be as low a value as is reasonably possible. To conform to these goals for a backplane having two or more signal routing layers, multiple slot positions and signal edge rates faster than approximately 5 ns cannot be efficiently implemented on a simple four-layer assembly. More layers are required.

There are many approaches to specifying the layer stackup of a backplane or ribbon cable assembly. Two common methods are presented here. These two methods *reflect a design methodology with specific concepts identified*, and they are not definitive. All design applications are unique and generally follow one of these two methods.

Method 1. Using Outer Layers as a Signal Routing Layer

When designing six or more layer backplanes, follow the guidelines presented in Chapter 4 using a reference plane adjacent to each routing plane. Connect ground planes to chassis ground (if required) in as many places as possible using a bypass capacitor as the interconnect method. Also provide for optional capacitive bypassing of the ground planes in as many locations as possible, in addition to all four edges of the board. Install these optional bypass capacitors between logic (signal return) and chassis ground *only* if required for EMI compliance or system functionality.

Method 2. Using Outer Layers as a Ground Plane

For high-speed, high-density, large-layer stackup (ten layers or more), RF common-mode eddy currents will be present between the PCB, the mounting bracket, the faceplate, and the backplane. The mating connector(s) between the backplane and mother-board generally contain a unique impedance with a value that may cause an impedance mismatch to occur between backplane and motherboard. Figure 7.3 illustrates this concept of impedance matching of a backplane-PCB-faceplate assembly and the RF loop currents developed by impedance mismatches between each interconnect.

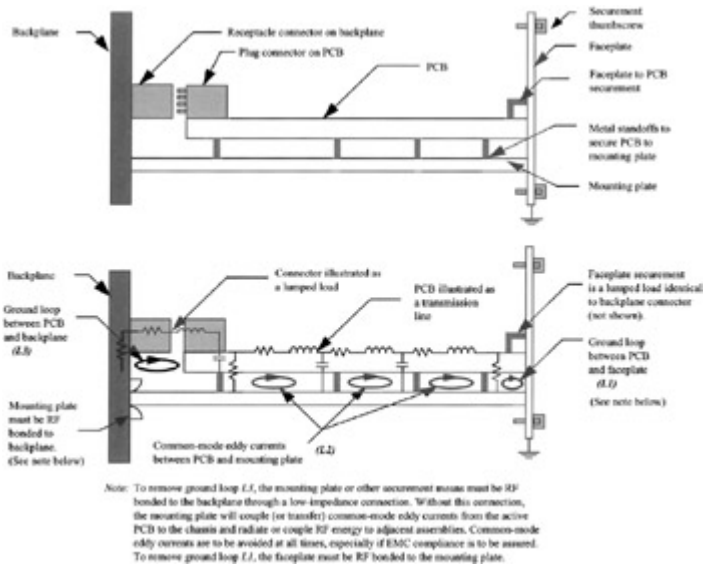

Backplane
Receptacle connector on backplane
Plug connector on PCB
PCB
Securement thumbscrew
Faceplate
Faceplate to PCB securement
Metal standoffs to secure PCB to mounting plate
Mounting plate
Backplane
Ground loop between PCB and backplane (L3)
Connector illustrated as a lumped load
PCB illustrated as a transmission line
Faceplate securement is a lumped load identical to backplane connector (not shown).
Ground loop between PCB and faceplate (L1)
(See note below)
Mounting plate must be RF bonded to backplane. (See note below)
Common-mode eddy currents between PCB and mounting plate
(L2)
Note: To remove ground loop L1, the mounting plate or other securement means must be RF bonded to the backplane through a low-impedance connection. Without this connection, the mounting plate will couple (or transfer) common-mode eddy currents from the active PCB to the chassis and radiate or couple RF energy to adjacent assemblies. Common-mode eddy currents are to be avoided at all times, especially if EMC compliance is to be assured. To remove ground loop L1, the faceplate must be RF bonded to the mounting plate.

Figure 7.3: Backplane interconnect impedance considerations.

Magnetic flux is developed internal to the interface connector owing to this impedance mismatch. This flux must be sourced (received) to chassis ground to prevent differential-mode RF fields from being developed. If the top layer of the backplane is a routing layer, magnetic flux within the connector can couple to signal traces on the outer layers of the PCB, creating an electric field potential. This newly created electric field potential in the backplane will now travel through the chassis (or card cage), allowing a differential-mode RF field referenced to chassis ground to propagate to other circuits, components, or free space.

If the top and bottom layers of the backplane, or daughter card, are a solid plane at *ground* potential, a lower impedance connection to *chassis* ground becomes available to both the backplane connector and faceplate screw securement. This low-impedance connector will now source RF currents to chassis ground, thus preventing ground loops L1 and L3 from existing between the faceplate to board and backplane to board, respectively. With solid bonding of the mounting plate to various locations on the PCB, ground loops L2 also become minimized, detailed in Fig. 7.3.

All signal routing layers must be routed internally (stripline), with both top and bottom layers being solid planes, preferably at AC chassis potential. If the outer layers are at 0V-potential, direct chassis connection from logic ground to chassis ground is easily achieved.

7.4.2 Number of Connector Slots

Determine the edge rate of the fastest clock or periodic signal trace that must travel throughout the backplane assembly. Calculate the maximum electrical length of these traces using the appropriate equations from Chapter 4 [Eq. (4.20) to (4.23)]. If there are many interconnects, measure the total physical routed distance between the two end connectors. Be sure to include the distance the signal trace must travel to on the adapter cards that plugs into the backplane or motherboard. Perform a worst case timing analysis to determine whether waveform degradation occurs because of capacitive coupling, when many connectors are provided. This is especially important if the physical spacing is electrically long between the two end connectors, relative to the source/load point on the adapter cards. Termination of signal lines is generally required with electrically long traces.

The greater the number of connector slots, the larger the value of lumped distributed capacitance presented to the circuit. With additional capacitance, degradation of signal quality can occur, sometimes to the point of nonfunctionality. Compensating for clock skew must be performed for all source drivers, taking into account the total capacitance of the routed trace as well as all loads present within the transmission line (discussed in Chapter 4).

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7.5 INTERCONNECTS

Concerns exist for interconnects used for backplanes, ribbon cable assemblies, and daughter cards, especially when a large number of connectors are provided. When many connector slots exist in an assembly, a summation of intrinsic device delay will occur between loads connected to the bus. This device delay is in addition to the intrinsic line delay when boards are inserted into the assembly. Our concern with signal delay is the capabilities of the total assembly related to I/O data transfer. I/O data transfer includes the source driver injecting a signal onto a bus, which must be received at a load located somewhere else.

An I/O connector must be chosen that is capable of handling edge rate transitions without degradation. To maintain signal integrity, the impedance mismatch at the connector boundary must be minimized. Sufficient ground and power pins must be provided throughout the connector to maintain a constant impedance throughout the assembly. An impedance mismatch causes common-mode RF currents to be capacitively coupled to adjacent signal pins. Differential-mode RF currents will then couple between signal and power/ground pins.

A backplane or daughter card connector used for high-speed applications must take into consideration the impact on signal transmission quality. Connectors, like signal traces and components, contain inductance, capacitance, and resistance.

Design techniques for interconnects using parallel routed traces involve

1. Keeping all trace route discontinuities as short as possible.

2. Using as many ground connections as possible within the allocated space or pinout. It is best to have one ground pin for each signal pin, which is not always feasible.

3. Establishing a common ground reference within the connector.

4. Using low dielectric constant board materials. The lower the dielectric value, the faster the velocity of propagation of the transmitted signal. Capacitance within a trace route will slow the transmitted signal, sometimes significantly. If we allow for a faster propagation medium, the "net result" is enhanced high-speed signal integrity using a faster dielectric, along with a slowing down of the transmitted signal due to line capacitance.

5. Maintaining the RF return path as close as possible to the signal path.

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7.6 MECHANICAL

If possible, one should try to provide additional real estate on a backplane for support circuitry. This additional area allows for filtering and termination of I/O connectors and hookup to the power supply. Decoupling, bulk and bypass capacitors, if required, are installed in this area. Cable shield (braid) attachment, if used, must also occur to all ground planes in this area through a low-impedance path to chassis ground, not logic ground or the power return plane. Low-impedance connection means a solid 360 degree bond to the metal I/O connectors, or a flat braid with a width to thickness ratio of 5:1, respectively.

All return and shield planes within a multilayer assembly must be RF bonded to chassis at every ground stitch location. The return plane is reference to the shield plane with a bypass capacitor. DC power and return connector pins should also be equally spaced within the connector to minimize RF ground loops that may be created by poor aspect ratios between pins, RF return path discontinuities, or poor trace routing. Signal traces, power, and ground pins should be at a maximum separation distance of 0.5 in. (1.27 cm). This distance is electrically optimal (transmissions length as a function of wavelength) in minimizing ground loops for most RF frequencies that are created by poor loop control. Traces must be routed between physically adjacent layers at 90 degrees (horizontal versus vertical routing). This routing requirement prevents crosstalk coupling between parallel planes, thus enhancing signal integrity.

To prevent crosstalk corruption between parallel trace routes, provision must be made for isolation or separation through use of the *3-W rule* between the traces (Chapter 4), or for adding guard (ground) traces on both sides of a critical trace route. This ground trace in reality enforces the *3-W rule*, while providing an alternative return path for RF currents, enhancing reduction of unwanted EMI developed within an interconnect assembly.

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7.7 SIGNAL ROUTING

Vias should be avoided when routing signal traces between planes for high-threat signals, which are defined as reset, clocks, audio, video, analog, high-speed transmission of data, and related signals. Each via adds approximately 1–3 nH inductance to the trace route. This inductance range is due to the physical characteristics of the via—diameter and length. Use of vias may make traces susceptible to signal integrity problems and EMI emissions. All traces must be routed on the same signal plane without use of vias, from source to load, if possible. Daisy-chaining traces is permitted only if load components are located adjacent to each other at the end of a long trace route. In all other cases, terminated radial trace routing (see Chapter 4) must be used. Series termination must be provided immediately adjacent to the output of each driver, with a minimal number of fanouts if this termination method is chosen. A radial termination maintains functional signal quality, as well as minimizing EMI noise by removing reflections within the transmission line, as well as minimizing overshoot and ringing.

When using I/O connectors and interconnects, it is important to minimize stubs, also identified as T-stub, or bifurcated traces, that sometimes occur during routing. T-stub lengths must be kept to a maximum of one-inch route on nonclock or nonperiodic signal traces. This length requirement may be increased based on the edge rate of the signal trace length. T-stubs are ***not*** permitted under any condition on periodic signal, high-threat, or clock lines. The key issue with T-stubs lies in signal integrity, which can lead to EMI concerns.

If a T-stub must be used because of problems with layout or routing, it must be as short as possible. Components must be relocated during layout to remove T-stubs created by an autorouter. A stub length should be no longer than the physical size of the device. For those applications where only a T-stub is possible, it is mandatory that both legs of the "T" be *exactly identical in length*. (*Note:* This is rarely a satisfactory approach). The measurement feature of the CAD system should be used to determine the routed length. If necessary, one must serpentine route the shorter trace until it achieves the desired length for signal functional reasons.

A potential or fatal drawback of using T-stubs lies in future changes to the PCB. If a different design engineer or PCB layout person makes a change to implement rework or a redesign, knowledge of a specific T-stub implementation may not be available. Accidental changes to a routed trace may occur, posing EMI and/or functionality problems.

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7.8 TRACE LENGTH/SIGNAL TERMINATION

For standard speed TTL logic, trace termination is generally not required. For higher speed components, terminators become mandatory. The bus driver (e.g., 74xxx244) on one plug-in board must be designed for driving terminated loads to other boards through all connectors located throughout a backplane assembly. The terminator, if used, must be the last load on a signal trace route, with the driver circuit the first item on the bus. If using multiple drivers from different slots, *high-current* drivers must be substituted for *high-speed* drivers. Furthermore, owing to the possibility of obtaining a distorted waveform, the slowest possible receivers, properly balanced and terminated, must be used.

Traces in backplanes must not exceed an RF electrically long length (related to the wavelength, edge transition times, and propagation delay of the clock signal). Hence, these traces must be as short as possible. Detailed discussion on calculating trace length and related concerns is presented in Chapter 4. This includes the length of a trace through a connector, which is measured from the source (component) to its farthest destination, including all stub lengths that are provided by adapter boards plugged into a backplane assembly.

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7.9 CROSSTALK

Crosstalk in backplanes, ribbon cable assemblies, adapter slots, and the like is a major concern for signal integrity and EMC compliance. This concern exists because many traces are routed in parallel and are generally spaced close together. Signal routes may be very short to extremely long (electrical wise with respect to propagation delay and signal edge rate transitions). With long trace routes, termination is required to remove harmful effects, thus enhancing signal quality. Although reference is made to ribbon cables within this section, the concepts are *identical* to backplane and daughter card implementation, as ribbon cable assemblies are easier to describe and illustrate.

The main concern with crosstalk, related to parallel traces, is to prevent electrical noise on one trace (source trace) from causing harmful interference to a victim trace. Three modes of propagation are observed when dealing with large bus structures: trace-to-trace, trace-to-assembly, and assembly-to-assembly coupling. When the term "return path" is used in this text, this subject can be considered as two layout techniques—one is providing a RF return path, and the other is enforcing the *3-W rule*. With wider trace separation, crosstalk is minimized.

Board-to-board interconnects are generally implemented by ribbon or flex cables, unless a backplane is provided for multiple board configurations. To accommodate a maximum number of signal conductors, engineers sometimes provide only a single return wire in the assembly and assign the rest of the interconnect pins as signal. This pinout assignment is poor, as the signal wire from the far edge of the return path will develop a significant differential-mode RF return loop. The result of this loop area allows the structure to radiate efficiently, along with crosstalk occurring between adjacent conductors. This configuration also is susceptible to externally induced ambients. These characteristics are present with an interconnect structure all the way down to a maximum physical separation distance of 1 in. (2.54 cm) end-to-end.

When using interconnects for backplanes, ribbon cables, or adapter cards, the optimal arrangement is to alternate transmission path traces between signal and 0V-reference, or ground. This is not desirable or feasible in most designs. The concept holds true for optimal performance but not in actual practice. One must make a tradeoff related to EMI and signal integrity/functionality based on the physical size permitted for the interconnect, cost of material, routing density available, and numerous other design concerns.

Three types of signal transmission configurations exist when crossing a boundary:

- A 0V-reference trace adjacent to each signal trace.
- One ground plane or RF return path adjacent to all signal traces in the assembly.
- Twisted pair ribbon cable.

Use of a shield partition between assemblies is desired when several ribbon cables are stacked against each other, which is typical in a multi-cable configuration. Although pleasing in appearance, system functionality and EMC compliance may not be achieved. Long cable routes allow

crosstalk to occur between parallel assemblies. With this situation, it is nearly impossible to determine where and how signal integrity problems or EMI occur.

Sample pinout configurations used to minimize crosstalk in parallel bus structures are illustrated in Fig. 7.4.

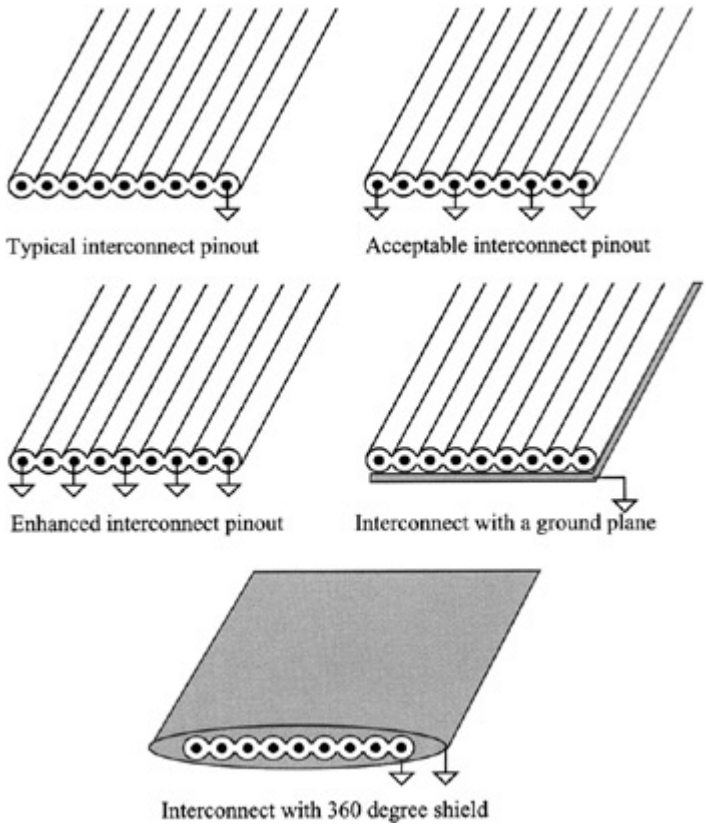

Figure 7.4: Preventing crosstalk using various interconnect configurations with parallel trace routes.

Note Although a ribbon cable assembly is detailed in Fig. 7.4, the same *concept* applies directly to backplane and daughter card interconnects to minimize or prevent crosstalk from occurring. The concept provided is to ensure that there are adequate RF return paths, separation of transmission lines, or placement of an image plane adjacent to each signal trace.

Performance of interconnects carrying high-frequency data is very susceptible to the configuration of the 0V-reference return. The most common layout procedure is to provide only one return pin, usually at the physical end of the assembly. This configuration creates a large inductive loop area for signals on opposite sides of the assembly. This is highly undesirable. If for some reason only one return path is provided, the recommendation is to locate this one path in the middle of the assembly. The most aggressive or sensitive signals must be placed adjacent to it. This design requirement is applicable only if one has the *luxury* of specifying a pinout configuration with multiple 0V-reference returns.

The preferred configuration to minimize crosstalk in a backplane or daughter card assembly is to provide a separate return for each signal (Fig. 7.4). This layout provides nearly optimal performance for EMI, while ensuring that a constant impedance transmission line route is available. The disadvantage of this configuration is the extra size of the layout and cost of implementation. An alternative layout technique is to provide one return path for every two signal traces. Although not as effective as one trace/one ground configuration, a smaller inductive loop area is present.

If a very large parallel route is required and the traces are electrically long, use of transmission line theory and application must be understood. For paired signals, crosstalk may be minimized by twisting the traces (similar to twisted-pair wire) internal to the PCB, if required. This technique is rarely used, as cost-effective data line filters are available that provide enhanced performance over this layout technique. Twisting traces is accomplished by routing a paired set of signals to a via pair, crossing the traces (on an adjacent routing layer), and with a second set of vias continue the signal route. An even number of twists is required for optimal performance. This outdated technique is shown in Fig. 7.5 and is provided for completeness. Twisting traces in a PCB is not feasible, consumes valuable real estate, and is an additional design concern during fabrication of the board. If twisting is used, many twists must be implemented as possible. The twist distance must be determined as $\lambda/20$ of the highest frequency (edge rate transition) that is expected to traverse the entire route from source to load,

regardless of how propagation occurs.

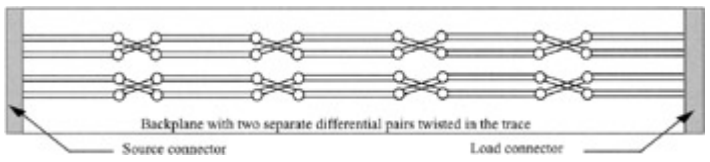

Figure 7.5: Differential pair twisting.

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7.10 GROUND LOOP CONTROL

If a one-, two-, or four-layer backplane is implemented, proper attention must be paid to minimize ground loops between all power and ground traces. Signal lines must be routed with as many ground paths as possible, interconnected to the main ground reference through the connector or interface. Power and ground must always be routed adjacent to each other (Fig. 7.6). This configuration is recommended for ribbon cable assemblies and may not be feasible for a typical PCB layout.

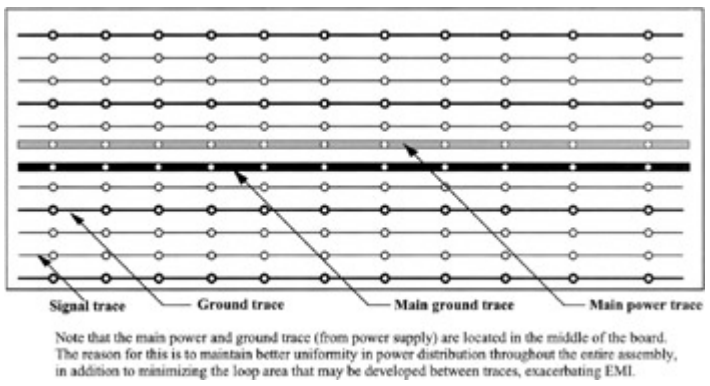
Signal trace
Ground trace
Main ground trace
Main power trace
Note that the main power and ground trace (from power supply) are located in the middle of the board.
The reason for this is to maintain better uniformity in power distribution throughout the entire assembly,
in addition to minimizing the loop area that may be developed between traces, exacerbating EMI.

Figure 7.6: Ground loop control in a backplane or ribbon cable assembly.

The easiest technique to prevent or minimize crosstalk is trace separation or bringing the RF return path as close as possible to the signal trace. Techniques include use of the *3-W rule* when traces are routed on the same plane or orthogonal (90°) when routed on adjacent signal planes (horizontal vs. vertical routing). Another technique for crosstalk control on the same routing plane between transmission lines is to separate parallel traces at a distance of 0.002 in. (0.05 mm).

As seen in Fig. 7.6, traces are routed in stripline fashion: signal trace adjacent to a ground trace. The main power and ground trace are routed in the middle of the board for better uniformity in power distribution. Also, routing power and ground adjacent to each other minimizes ground loops in the power section of the backplane. Use of many ground traces in a backplane or ribbon cable minimizes development of crosstalk between traces. This separation for high-speed, high-threat signal traces (source) prevents corrupting other sensitive traces (victim), such as reset, alarm, video, audio, and analog control.

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7.11 GROUND SLOTS IN BACKPLANES

A common practice when designing backplanes is to select a connector with pressfit (stake) or through-hole pins. Newer technology connectors with a large number of pins are available in surface mount form. Surface mount connectors route signal traces to inner layers through vias. Depending on the connector style and method chosen, ground slots may be accidentally designed into the backplane assembly.

A ground slot is a continuous discontinuity along the length of the connector (Fig. 7.7) within the layout software program. A ground slot is created because clearance holes for the pins of the connector, or vias, are larger than they need to be. These clearance holes overlap each other, creating a continuous discontinuity within the plane. There must be sufficient distance between pins for routing traces, which makes this layout method appear to be acceptable when visually viewing the layout with the power and ground plane layers turned off. Adjacent to each routing layer must be a power or ground reference plane used not only for power connection, but also for signal return of RF currents (image plane). With large overlapping cutouts on all layers of the assembly, these solid planes will have discontinuities that prevent RF currents from returning to their source in a low-inductance, straight-line manner. Under this situation, crosstalk may still occur owing to the mutual inductance that exists between traces sharing a common signal return path. In addition, inductance added to the trace may develop unwanted common-mode currents, while degrading the edge rate of clock signals propagated between boards at opposite ends of the backplane.

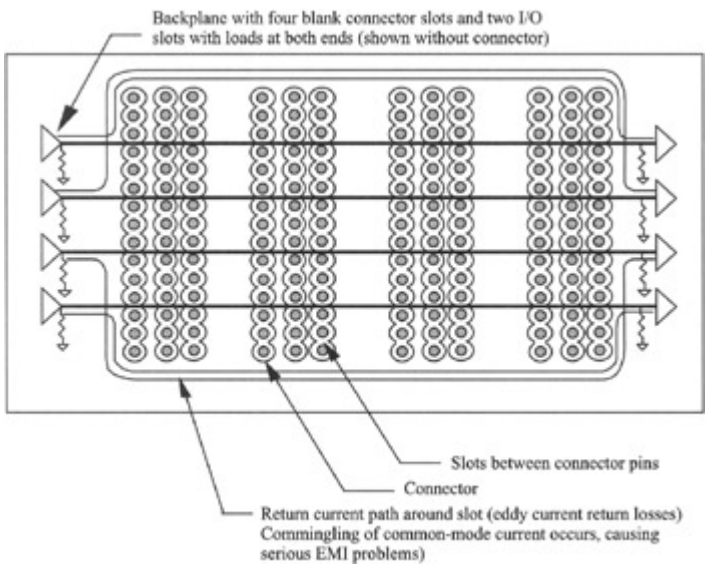
Backplane with four blank connector slots and two I/O slots with loads at both ends (shown without connector)
Slots between connector pins
Connector
Return current path around slot (eddy current return losses)
Commingling of common-mode current occurs, causing serious EMI problems)

Figure 7.7: Ground slots in a backplane or parallel bus structure.

As seen in Fig. 7.7, return currents between adapter modules cannot mirror image themselves directly under their respective trace route. Instead, RF return current is diverted to the ends of the connector assembly due to a continuous slot created by oversized holes. To remedy this problem, a solid reference plane with sufficient copper must exist around all through-hole locations.

Figure 7.7 also shows that RF return current from traces parallel to each other actually overlaps at the edge of the through-hole slots. The commingling of RF return current creates a situation of common-mode impedance coupling. This means that RF current from one return path will mix with other return current sharing the same physical space. Depending

on the phase of the RF current for each trace, a significant amount of RF energy may be present, exacerbating EMI harmful effects.

The additional inductance added to a trace, traveling around the ground slot is calculated as

(7.1)
$$L = (5\,d)\,ln\left(\frac{d}{w}\right)$$

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where L = inductance, nH
w = trace width (in. or cm)
d = slot length of connector (in. or cm)

The value of d is the extent of current diversion away from the signal trace. Consistent units of measurements must be used.

Inductance is not related to the width of the ground slot; it is related only to the perpendicular length of the slot. Any slot length will cause RF diversion. Since RF current division is based only on slot length, traces closest to the edge of the connector will have less current diversion than traces routed in the middle of the connector (longer return current travel length).

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[6] Williams, T. 1996. *EMC for Product Designers.* 2nd ed. Oxford, UK: Butterworth-Heinemann.

[7] Moongilan, D., and T. Palaniswamy. 1999. "Backplane Grounding Models for Controlling Common-mode Noise and Radiation." *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility,* New York: IEEE, pp. 212–217.

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Chapter 8: Additional Design Techniques

8.1 LOCALIZED PLANES

During component placement, oscillators, crystals, and support circuitry (buffers, drivers, etc.) must be located over a single localized plane. This plane is usually at ground potential but can be at voltage potential. Some components, having unique power requirements, mandate a voltage plane directly under the device. Regardless of potential, the concept described herein is the issue of importance: localized planes. This localized plane is located on the outer microstrip layer and ties directly into the main power or ground planes of the PCB through both the oscillator and component's power and ground pins. In addition to these pins, a minimum of two additional vias is required. If the plane is at ground potential, it should be positioned next to a ground stitch location, where it must be fully connected in a 360° fashion to remove RF energy present within the plane. Use of soldermask is not recommended. Soldermask provides a dielectric material on the board that could possibly change the impedance of a transmission line that carries the clock signal, thus causing potential concerns about signal integrity. This situation rarely occurs, however, and should not be a significant design concern. An example of a localized plane at ground potential is shown in Fig. 8.1.

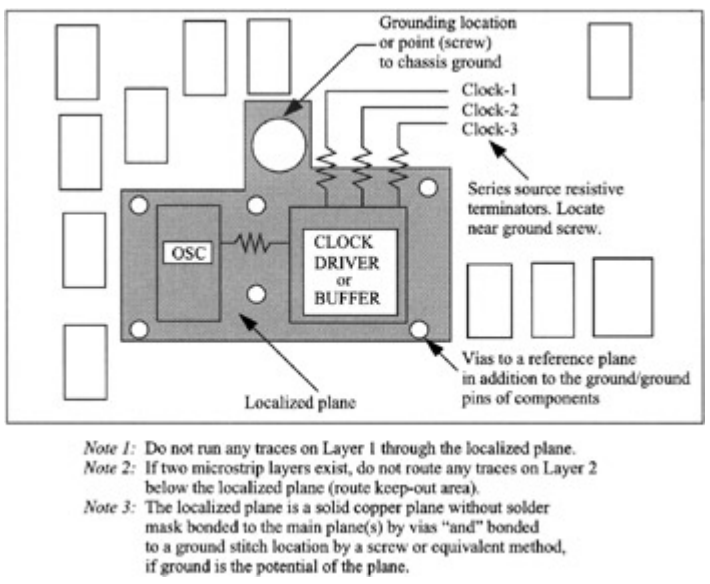
Grounding location
or point (screw)
to chassis ground
Clock-1
Clock-2
Clock-3
Series source resistive
terminators. Locate
near ground screw.
OSC
CLOCK
DRIVER
or
BUFFER
Vias to a reference plane
in addition to the ground/ground
pins of components
Localized plane
Note 1: Do not run any traces on Layer 1 through the localized plane.
Note 2: If two microstrip layers exist, do not route any traces on Layer 2
below the localized plane (route keep-out area).
Note 3: The localized plane is a solid copper plane without solder
mask bonded to the main plane(s) by vias "and" bonded
to a ground stitch location by a screw or equivalent method,
if ground is the potential of the plane.

Figure 8.1: Localized plane (ground potential).

There are a number of reasons for using a localized plane in clock or frequency generation areas:

- Circuitry inside the oscillator creates common-mode RF currents. If the oscillator package is a metal can, the DC ground pin must be relied upon for both DC voltage reference and a path for RF currents to be sourced (or sunk) to ground from the oscillator circuitry. Depending on the type of oscillator chosen (CMOS, TTL, ECL, PECL), RF currents created internal to the package can become excessive. The ground pin is unable to source large amounts of *LdI/dt* current (*L* from the pin lead and internal bond wire) to ground. The nearest image or reference plane (internal to a multilayer stackup) is generally two or more layers away. This physical distance spacing may be excessive, relative to the magnitude of magnetic flux generated from the oscillator; it is thus

inefficient as a coupling path for flux cancellation of RF common-mode currents to ground.

- If the oscillator is a surface mount device, the situation mentioned above is made worse because SMT packages are usually plastic. RF currents created internal to the package will radiate into free space and may couple to other components or cable assemblies located nearby. The high impedance of the PCB material, relative to the impedance of the reference pin of the oscillator, prevents RF currents from being sourced to ground in an optimal, low-impedance manner. SMT packages will always radiate more RF energy than a metal encapsulated case.

- Placing a localized plane under the oscillator and clock (frequency generating) circuits provides an image plane that captures common-mode RF currents generated internal to the circuitry, thus minimizing radiated RF emissions. This localized plane is also "RF hot." To prevent differential-mode RF energy that is also sourced to the localized plane, multiple connections to all system reference planes must be provided, if ground is the potential of choice. Vias from the localized plane will provide a lower impedance path to ground than a single, high-impedance pin designed to operate as a 0V-reference source. To enhance the performance of this localized plane, clock generation circuits should be located adjacent to a chassis ground stitch connection. This localized ground plane must be connected to a plated through-hole, 360 degrees. A low-impedance RF bonding connection to ground must exist. Connection by one or more traces (wagon wheel style) to a ground stitch location can defeat a low-impedance connection. While thermal relief "wagon wheel" connections are sometimes acceptable, they also degrade the performance of the connection by providing a higher level of inductance to source currents to ground owing to the small trace width that connects the plane to the plated through-hole.

- When using a localized plane, no traces are to be run through this plane! If a trace travels through a localized plane, the potential for small ground loops or discontinuities exists for the trace that violates this plane. This ground loop can generate problems for higher frequencies. Why install a localized plane when you defeat its functional use by running traces through it? In addition, if a trace is routed through this area, capacitive coupling of common-mode energy from the clock-generating components can occur, thus causing disruption to the unwanted trace through the process of crosstalk. If one routes a reset line running directly under an oscillator, the design engineer will spend considerable time figuring out why this product keeps resetting.

- Support circuitry (clock drivers and buffers) must be located adjacent to the primary oscillator. This localized plane must be extended to include all components. Generally, an oscillator drives a clock buffer, which is usually a high-speed, fast-edge-rate device. Because of the functional characteristics of these drivers, RF spectral currents will be developed at harmonics of the primary clock frequency. When using CMOS components, with a +5V swing and a low-impedance transmission line (PCB trace), drive current can become excessive. The level of electromagnetic energy (power: $P_{rf} = V_{rf} I_{rf}$) injected into the trace will cause common-mode and differential-mode RF currents to be propagated as either radiated or conducted emissions. These currents can cause signal integrity problems (crosstalk) and possible noncompliance to EMC requirements.

8.1.1 Localized Decoupling Capacitor Implementation

A unique benefit of localized planes is the ability to develop, at no cost, additional decoupling for specific components. A capacitor, by definition, is two parallel plates separated by a dielectric. As discussed earlier, a localized plane can be at either voltage or ground potential, application specific. Because a large plane is incorporated on the outer layer of the PCB directly under a component, the ability to add more decoupling into the artwork is a simple matter of implementation.

Assume a localized plane is on the top layer at ground potential. Immediately on the next layer within the stackup (Layer 2), a second

localized plane at *voltage* potential is incorporated. If this second layer is a solid reference plane at one potential, select the potential that is opposite the localized plane. For example, if the localized plane is at ground potential, Layer 2 is a power plane. However, if the layer is an embedded microstrip routing layer, the area directly below the localized plane becomes a route keep-out zone for this layer only. It is never desirable to route traces directly under frequency-generating components, as RF fields from components can, and will, capacitively couple to the routed traces, causing crosstalk or signal integrity concerns to develop.

An example of several configurations of localized decoupling is presented in Fig. 8.2 to illustrate implementation. The value of the localized capacitor is calculated by Eq. (3.6): $C_{pp} = k(\epsilon_r A/d)$ Once we know the capacitance value, determination of the effectiveness is possible, associated with stored energy capabilities. The self-resonant frequency of the capacitor is extremely high, as there is virtually no lead-inductance in the assembly to lower the self-resonant frequency. The impedance, being very low, provides a very rapid delivery of electrons to the component during a logic state transition.

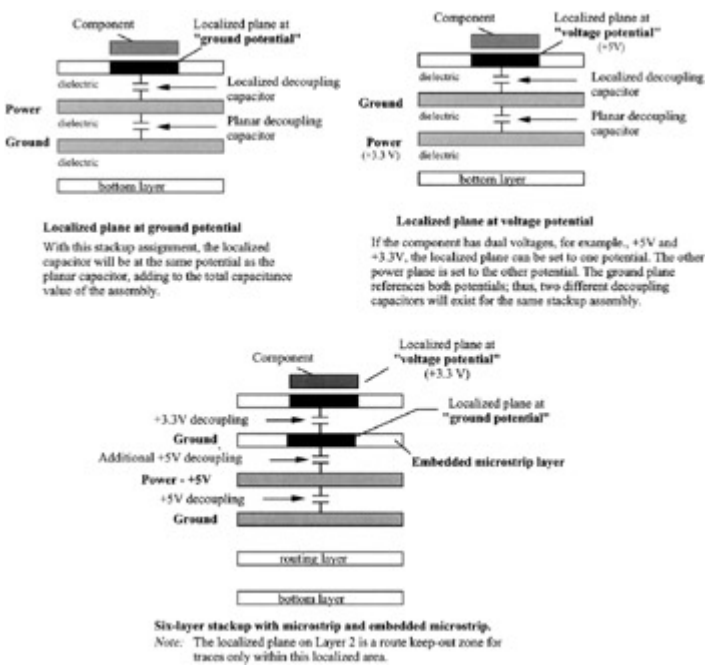
Component
Localized plane at "ground potential"
dielectric
Localized decoupling capacitor
Power
dielectric
Planar decoupling capacitor
Ground
dielectric
bottom layer
Localized plane at ground potential
With this stackup assignment, the localized capacitor will be at the same potential as the planar capacitor, adding to the total capacitance value of the assembly.
Component
Localized plane at "voltage potential" (+5V)
dielectric
Localized decoupling capacitor
Ground
dielectric
Planar decoupling capacitor
Power (+3.3 V)
dielectric
bottom layer
Localized plane at voltage potential
If the component has dual voltages, for example., +5V and +3.3V, the localized plane can be set to one potential. The other power plane is set to the other potential. The ground plane references both potentials; thus, two different decoupling capacitors will exist for the same stackup assembly.
Component
Localized plane at "voltage potential" (+3.3 V)
+3.3V decoupling
Localized plane at "ground potential"
Ground
Additional +5V decoupling
Embedded microstrip layer
Power - +5V
+5V decoupling
Ground
routing layer
bottom layer
Six-layer stackup with microstrip and embedded microstrip.
Note: The localized plane on Layer 2 is a route keep-out zone for traces only within this localized area.

Figure 8.2: Localized decoupling capacitor implementation built internal to a board stackup.

Use of localized decoupling is appropriate for components that consume a large amount of current required for optimal operation. In addition, if common-mode energy is present within the silicon die, the localized plane will capacitively shunt the RF energy into the 0V-reference system, away from circuits easily corrupted by radiated fields.

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8.2 20-H RULE

RF current will radiate off the edges of the PCB because of interplane coupling between the power and ground plane owing to magnetic flux linkage. This interplane coupling is called *fringing* and is generally observed on only very high-speed PCBs. When using high-speed logic and high-frequency clocks, the power and ground planes can couple RF energy to each other, thus radiating this energy into free space and the environment. To minimize this coupling effect, all power planes must be physically smaller than its closest ground plane per the *20-H rule*.

Figure 8.3 shows the effects of RF fringing from the edge of a PCB and illustrates how magnetic flux exist. The two planes are first located far apart and then are brought in close to each other. To visualize what happens, consider a source of current modulation, along with any other impedance that may be present. This current source can be developed by an item such as a storage capacitor, positioned in various places throughout the PCB. For example, a component is on one side of a plane, and the DC current source (storage capacitor) is on the exact opposite side. There will be a clearly defined current and flux pattern within the planes. Under this condition, and without flux linkage between the planes, the current and flux "loop" will take a defined form. Flux will surround each plane, appearing, in general, more or less elliptical.

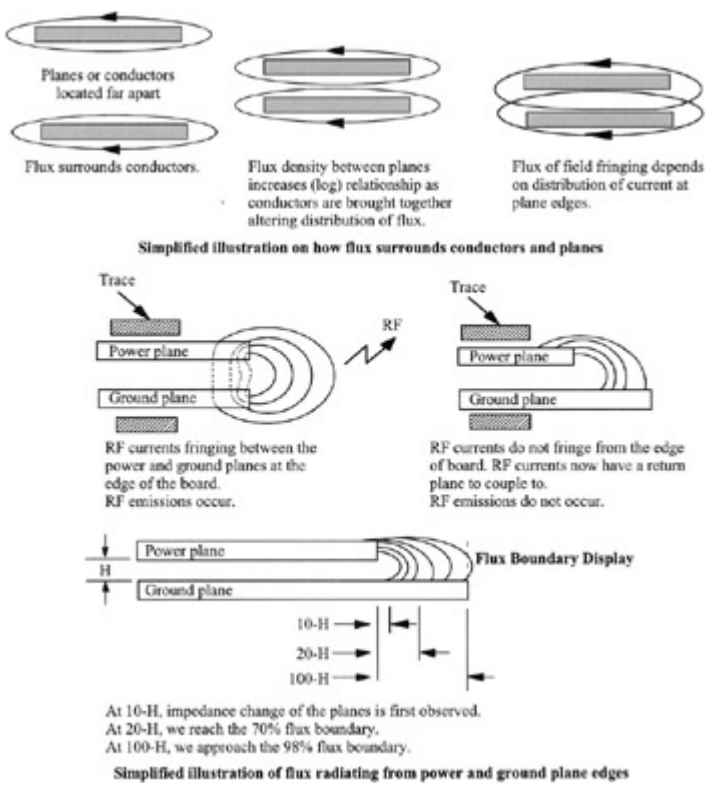
Planes or conductors located far apart
Flux surrounds conductors.
Flux density between planes increases (log) relationship as conductors are brought together altering distribution of flux.
Flux of field fringing depends on distribution of current at plane edges.
Simplified illustration on how flux surrounds conductors and planes
Trace
Power plane
Ground plane
RF
RF currents fringing between the power and ground planes at the edge of the board.
RF emissions occur.
Trace
Power plane
Ground plane
RF currents do not fringe from the edge of board. RF currents now have a return plane to couple to.
RF emissions do not occur.
H
Power plane
Ground plane
Flux Boundary Display
10-H
20-H
100-H
At 10-H, impedance change of the planes is first observed.
At 20-H, we reach the 70% flux boundary.
At 100-H, we approach the 98% flux boundary.
Simplified illustration of flux radiating from power and ground plane edges

Figure 8.3: RF fringing effects from power and ground planes.

Now slowly bring the two planes closer together. As the flux begins to link, the flux density is significantly increased between the planes. In order for the flux density to increase, the "shape" of the "elliptical" flux changes—it is directed inward toward the opposing plane. Two things happen in this process, other than the increase of flux density between planes: (1) the "shape" of the flux that surrounds the planes gets directed inward; and (2) the fringing of the flux at the edges of the planes gets directed outward.

Use of the *20-H rule* increases the intrinsic self-resonant frequency of the PCB, because the physical dimensions of the power distribution network are altered. Since less capacitance will be present, there will be a higher

self-resonant frequency of operation. This impedance change in the power distribution threshold is first noticed at approximately *10-H*, with *20-H* representing the approximately 70% flux boundary. The dimension "H" is the physical distance spacing between the power and ground plane within the stackup. Flux boundary refers to the distance that magnetic lines of flux are observed from the planar structure in the near field. To achieve a 98% flux boundary, *100-H* is used. Increasing the physical dimension between planes greater than *20-H* does not provide any significant reduction in the propagation of RF energy and in fact makes the PCB more difficult to route.

To implement the *20-H rule*, determine the distance spacing between the power plane and its nearest ground plane. This distance spacing includes the thickness of the core or prepreg, including isolation separation specified in the PCB fabrication drawing. Assuming a distance separation of 0.006 in. (0.2 mm) between the power and ground planes, calculate H as [20 * 0.006 in. (0.2 mm) = 0.120 in. (3.0 mm)]. Physically make the power plane 0.120 in. (3.0 mm) smaller than the ground plane. Should a power pin to a component be located inside this isolated (absence of copper) area, the power plane may be altered to provide power to this pin by using a trace or by altering the shape. This alteration of the power plane is shown in Fig. 8.4. Altering the shape of the reduced power plane does not affect performance.

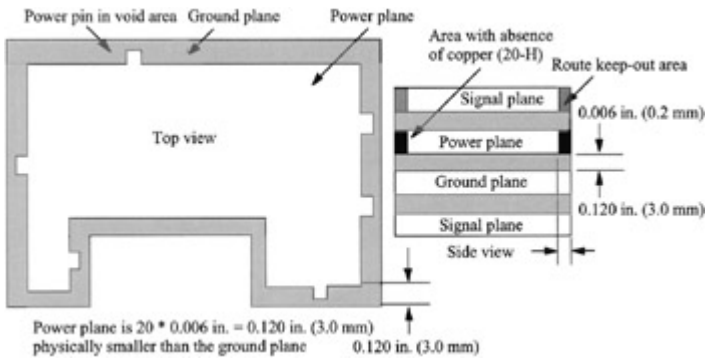
Power pin in void area
Ground plane
Power plane
Area with absence of copper (20-H)
Route keep-out area
Top view
Signal plane
Power plane
Ground plane
Signal plane
0.006 in. (0.2 mm)
0.120 in. (3.0 mm)
Side view
Power plane is 20 * 0.006 in. = 0.120 in. (3.0 mm) physically smaller than the ground plane
0.120 in. (3.0 mm)

Figure 8.4: Implementing the 20-H rule.

When using the *20-H rule*, any traces on the adjacent signal routing plane, located over the absence of copper area, *must* be rerouted inward to be physically adjacent to the solid power plane, with no exceptions. It becomes important now to check two or more planes for proper implementation: *20-H* on the power plane, and routing of traces over a solid power plane. Traces cannot be routed on the outer edge of the routing layer adjacent to a physically smaller power plane because traces must be adjacent to a reference plane for impedance control and for RF return current. Routing traces in this area gives identical results to routing a trace over a moat (violation), as discussed in Chapter 5.

If functional partitioning is required within the PCB, *20-H* should be implemented in high-frequency bandwidth areas only (e.g., CPU, video, Ethernet, SCSI, LAN interfaces, and other high-speed circuits). When providing isolation and filtering between digital and analog sections, or equivalent circuits, the *20-H rule* is applicable (Fig. 8.5).

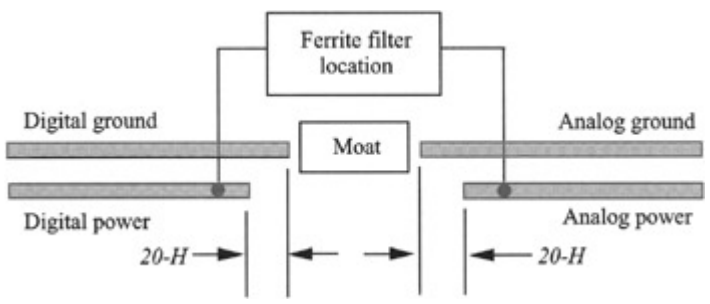

Figure 8.5: Application of the 20-H rule and power plane isolation.

Although use of *20-H* is required for high-speed components and high-bandwidth sections, at times this design technique is *not* appropriate and, in fact, is not recommended. This concern lies with the physical dimensions of the PCB related to RF wavelength of energy that may be present. Equation (2.6) can be used to calculate the wavelength of a signal ($\lambda = C/f$), where λ = wavelength, C = velocity of propagation in the media where the energy is contained (not generated), and f= frequency (MHz). With this value, we discover that the physical dimension of a RF wave may be

physically greater than the physical dimensions of the PCB. When this occurs, use of the *20-H rule* provides no benefit.

For example, if a 100-MHz signal is provided, the physical RF dimension is λ = 9.84 in. (24.99 cm). Various combinations of wavelength that would be observed as radiated emissions include λ/4 = 2.46 in. (6.25 cm), and λ/8 = 1.23 in. (3.12 cm). If the physical dimensions of the PCB are 5 square in. (12.7 cm), use of the *20-H rule* is not appropriate. The physical dimensions do not match any wavelength or variation of wavelength to the signal. Use of *20-H* must be determined *independently* for each individual edge of the board, where the straight-line linear dimension equals that of any permutation *or* wavelength of all clock frequencies present.

Technical Presentation on How and Why the 20-H Rule Works

Note The intended audience for this book is practicing engineers with hands-on requirements to get the job done. The following discussion is extremely technical.

In practical conditions, in the manner in which current circulates within/between the power and ground planes, use of the *20-H rule* can improve (increase) the self-resonance of circuit boards. There are conditions to the validity of using the rule. All that is required is an understanding of how fields and flux appear at the edges of a PCB. Power and grounds are in reality, transmission lines, the same as a typical signal trace that requires termination.

Analysis of a Microstrip Transmission Line

The first item to consider is the physical shape of current density distribution between a microstrip layer and how RF fields propagate within this transmission line. For this configuration, the return image of the RF current follows directly under the trace in a channel that ranges for signal currents between *3-W* and about *10-W* (*W* is the width of the trace). This distribution shape changes, depending on the percentage of the flux and field boundary between the signal and reference plane. This flux and field-coupling channel defines the physical characteristics (shape) of the RF current distribution. Consequently, the RF current and line geometry of the image flux will always be directly under the line; that is, it follows this pattern, no matter what the exact trace routing shape becomes.

For a microstrip trace, it is mandatory to prevent signal flux and RF return current from perturbations in the reference plane or return path, such as vias. The same is true for traces routed exactly at the physical edge of a reference plane. If poor trace routing occurs, the return flux image will not be uniform, and will have to circulate around the discontinuity. This circulation around the discontinuity causes a skew in the return image, or propagation off the planes at the edge of the board resulting in a partial loss or capture of the RF return image. For this situation, EMI will be impacted, yet signal integrity is still assured.

The location of terminators in any transmission line is very important. For example, assume a transmission line where termination is not located at the end of the trace route. Suppose that regardless of line length, termination is located about 30% (just for an example to consider) down the transmission line (Fig. 8.6). This figure also illustrates both the electrical and mechanical representation of a power and ground plane as they relate to a transmission line equivalent circuit.

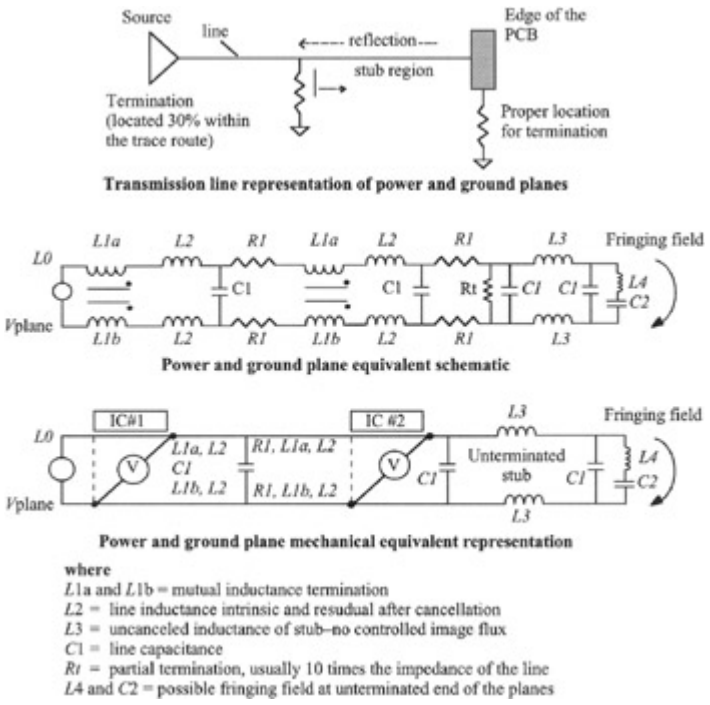

Figure 8.6: Transmission line equivalent circuits of the power and ground planes.

Assume that the termination value is about ten times higher than the characteristic impedance of the transmission line. In this situation, the "termination" is a value that will *not* fully terminate the line. The position of the termination is such that a rather long "stub," as a percentage of total transmission line length, is created at the end of the line. The flux field fringing depends on the exact relationship and distribution path near the plane edges. The distribution of the flux depends on the geometry of the component and its geometry from the edge of the PCB.

The result of this example is that the transmission line will not be properly terminated. The stub will create reflections back toward the source that can set up resonances in the line. The reflections themselves will only be partially terminated, because the impedance of the termination is incorrect (too high).

Analysis of Planar Application: Plane Terminations

> For whatever reason, the transmission line symmetry-relationship between planes in the *z*-axis seems to be difficult for many to realize, at least in terms of visualization. As in linear transmission lines, planes offer "stubs" in regions where they are "not" terminated. These stubs cause reflections and self-resonances throughout various circuit boards.

Next, translate transmission line theory to the power and ground planes, along with their respective currents contained between the two planes. What is the "shape" of the current flow? Obviously, it depends on the positions of the loads. The shape or geometry of the flux lines, as well as the manner in which the current propagates between planes is difficult, if not impossible, to simulate for a fully active PCB with many components and routed traces switching current levels simultaneously.

A PCB with a source injected into the center of the board will have current travel to the edge of the board in all directions (360 degrees). This current flow is an excellent example of a complex problem that is not well understood by engineers. This analysis is simply an application of the microstripline analogy given earlier, viewed now with the planes forming the transmission line in a vertical, or *z*-axis.

Assume a source located at the center of a PCB is simulated using field solvers. Under the circuit is a small loop area between the ground and power pins where the current between the pins is circulating. The current circulating in the small loop area, including the position of the bypass capacitors, can be very high. This flux and fields from this component are circulating, defined by the shape of the layout and the pinout of the device itself.

The planes, however, continue out far beyond the shape of this boundary. This simply means that they are "not" terminated, and if they are "not" terminated, the planes become one *large* planar "stub" that causes reflections and resonances throughout the board. These resonances

usually do not cancel because of the phase angle skew between the planes. This skew is caused by the inductive characteristics of the planes.

In any transmission line, there are two possible solutions to this problem. Either plane (usually the power plane) could be "undercut" to mechanically "remove" the stub; or the edges of the plane could be terminated in a distributed manner. Since the planes themselves are distributed, terminations would have to be located around the perimeter in small increments, being bandwidth and harmonic spectra dependent. In addition, when attempting to "edge-terminate" transmission lines, which are in fact "the planes," there exist a spectra of RF energy at different wavelengths. This spectral energy is observed because the planes are of significant size with respect to wavelength harmonics. Multiple and frequent terminations around the edges will be required. These terminators must be located at intervals that are small with respect to the spectra of interest.

The advantage of undercutting one of the planes, usually the power plane, is that power energy is not wasted in the dissipation of the terminations. RC terminations can be poor at specific frequencies of concern, because of the resonance of the capacitor and the connection traces.

In this discussion on transmission line theory, two rules are to be noted when implementing *20-H*. First: "no flying unterminated-stub power planes!" If these planes were viewed as linear transmission lines, one would immediately visualize this problem. For this reason, planes in the *z*-axis, the unterminated stubs, seem to be more difficult to realize. This visualization is difficult, because they are designed to operate in low (ohmic) value impedances that are appropriate for power distribution. Because of this low ohmic impedance, the planes would require low ohmic values of termination impedance, which increases drive current-a highly undesirable side-effect.

Second, because of power circulation from components, determine where the device is located, *relative* to the "edge" of the PCB. *Undercut* the power plane away from the edge to the point where the transmission lines, which are in fact the planes, are brought to the point of the termination of the RF current—just like a *z*-axis version of the *3-W rule*. In many situations, assuming power plane separations of 5 mils, one must undercut to terminate the "planar line" at approximately 100 mils, or about 20 times the height of the planes. This is simplified as *20-H*.

The intended goal of the *20-H rule* is to terminate the planes locally toward the circulating current boundaries of the flux and RF fields formed by device-power-currents located at the edges of the boards, not to set an arbitrary dimension. Even if one were to resistively terminate the "flying" (unterminated) planes, the mechanical geometry of the resistors (at least 1206 in size) would probably require undercutting the planes about *20-H* at a 0.055 in. (1.4 mm) planar height.

The propagational model, as an antenna structure for the power planes, can take several forms ranging from a slot antenna formation at various frequencies to a dipole resonance at others. The form of the antenna model depends primarily on the configuration of the power current propagational circulation; where and how the planes are terminated. The location of the formations/circulation with respect to the three axes of the circuit boards needs to be converted.

To summarize, if the planes are properly considered as *z*-axis transmission lines, with stubs that require removal (undercutting) or termination, the performance of boards particularly in terms of resonances can be improved dramatically.

As a point of interest, one major computer company found the technique so effective that it attempted to patent it in the United States Patent Office as a design technique.

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Chapter 8 - Additional Design Techniques

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

IEEE Press © 2000

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8.3 TRACE ROUTING FOR CORNERS

Attention to detail must be observed when designing with sub-nanosecond transitions to avoid an effect similar to capacitive loading that occurs during normal routing of traces. When a trace makes a bend on the PCB, its capacitance per unit length will increase while its inductance per unit length will decrease. This is shown in Fig. 8.7 and is true for sharp angles of 90° or more. The magnitude of the capacitive and inductive change within a sharp-angled corner is extremely small.

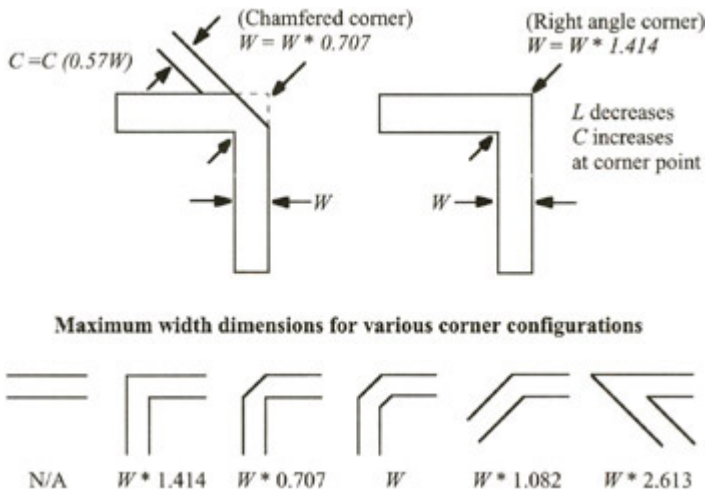

Figure 8.7: Corner configurations.

A corner increases in capacitance and decreases in inductance because of the physical shape of the corner. If the corner is a pure 90°, the width of the trace at the corner, W', is equal to $W' = W * \sqrt{2} = W * 1.414$. This is shown in Fig. 8.7. The magnitude of this inductance change is *only* for the finite dimension that is presented to a propagating signal. Regarding capacitance, when two parallel plates are provided with a dielectric material, a capacitor exists. Because there is a tiny bit more copper at the corner, owing to the additional width, capacitance increases. This increase is based on the trace corner (one capacitor plate) referenced to a plane (the other capacitor plate). A capacitive load will round off or change the edge rate of a signal trace. Now comes the real item of concern—the *magnitude* of disruption that the corner really has on a propagating signal.

Figure 8.7 illustrates various corner configurations. The dimension *W* for six configurations in the bottom of the figure illustrates the actual width of the corner, measured along the center axis from the inside corner to the outer corner.

Rounding the outside corner of the bend leaves a constant width dimension that is physically smaller than a sharp 90° or a chamfered 45° angle. Any edge that is less than 90° will reduce the amount of reflections and edge transition degradation for signals traveling through the corner. When the corner is chamfered (45° angle), a reduction of up to 57% of the capacitance is achieved because a portion of the corner width has been removed; there is less copper on one plate of the capacitive structure.

In order to discuss the magnitude of effect from right-angle corners in a PCB layout, the following is examined [2].

8.3.1 Time Domain Analysis

When performing time domain analysis, it is necessary to determine

whether an impedance mismatch will cause a signal integrity or emissions problem. This concern lies with the known fact that there will be a change in Z_o, the characteristic impedance of the trace. This change is described by Eq. (8.1) to determine whether the impedance at a corner using a particular routing geometry will cause a functionality concern. When a signal propagates through a transmission line, it does so at a specific velocity of propagation. The speed of an electromagnetic wave through a dielectric material with an effective relativity permittivity, ϵ_r of 4.3 (typical value of FR-4 at 1000 MHz) for microstrip topology is 1.65 ps/in. (4.19 ps/cm) and 1.43 ps/in. (3.63 ps/cm) for stripline. As observed, the trace that is routed stripline propagates slightly slower than microstrip. This slower propagation is due to the transmission line being completely surrounded by a dielectric material, whereas microstrip has approximately 50% of the dielectric consisting of air.

(8.1)
$$Z = \sqrt{L/C}$$

➡ Get MathML

The primary electrical effect, in the time domain for a right-angle corner referenced to a plane, is a small amount of parasitic capacitance to ground, described by Eq. (8.2) [3]. For example, assume Z_o = 65 ohms (typical impedance of a PCB trace), ϵ_r = 4.3, and W = 0.007 in. The right-angle corner has a capacitive *increase* of C = 0.014 pF or 14 femtoFarads, a value that is so small as to not cause concerns for signals propagating through the transmission line below 100 GHz.

(8.2)
$$C = \frac{61 * W \sqrt{\varepsilon_r}}{Z_o}$$

➡ Get MathML

where W = width of line (inches)

ϵ_r = relative permeability, compared to air

Z_o = characteristic impedance of the trace (ohms)

C = loaded capacitance of the corner (pF)

The 10–90% rise-time constant (edge transition rate) associated with a right-angle corner is described by Eq. (8.3) [4].

(8.3)
$$T_{10-90\%} = 2.2\left(\frac{61W\sqrt{\varepsilon_r}}{Z_o}\right)\frac{Z_o}{2} = 67W\sqrt{\varepsilon_r} \quad \text{ps}$$

➡ Get MathML

Equation 8.3 tells us that the only signals affected by a trace width discontinuity (right-angle corner) are for signals with an edge rate transition faster than 100 ps. In reality, the actual edge transition speed, before signal integrity concerns develop, is 50 ps. The 50 ps value is conservative for design purposes. Once we start to have signals with this fast transition time, the product is probably operating in the GHz range, using microwave design and layout techniques, which mandate use of round corners anyway, for all traces.

Research [2] on various corner configurations (Fig. 8.8) was performed to ascertain the magnitude of disruption to a propagating wave when used in an actual environment, not simulated. A typical plot of the impedance discontinuity of a right-angle corner is detailed in Fig. 8.8.

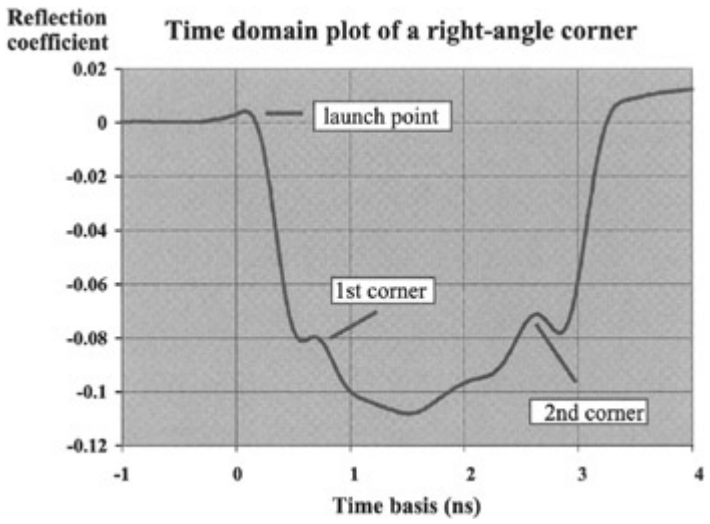

Figure 8.8: Time domain plot on effects of a right-angle corner. Two corners located within an 18-inch (47.7 cm) trace route.

The reflection of the signal, as measured at the launch point, is known as the reflection coefficient, ρ_s, defined by Eq. (8.4). The test trace had two right-angle corners in close proximity; hence, the time duration of the pulse in the plot reflects these two corners. The actual time period of the corner discontinuity is approximately 15 ps. When using the reflection coefficient equation (actual impedance of the trace and load), Eq. (8.4), we are looking at only one-half of the reflected wave, since round-tip propagation must occur for functionality reasons.

(8.4)
$$\rho_s = \frac{Z_s - Z_o}{Z_s + Z_o}$$

Get MathML

where ρ_s = reflection coefficient

Z_s = output impedance of the driver (ohms)

Z_o = characteristic impedance of the trace (ohms)

The effect that a right-angle corner has on the characteristic impedance of the trace, Z_o, will decrease the total trace impedance by approximately 15 to 20% *only* at the finite point of the sharp corner. Most PCBs are designed to have a tolerance of ± 10% owing to the manufacturing process. A very small functional glitch may affect trace impedance for a finite time within the transmission line. This impedance discontinuity will last for approximately 15 ps per corner. Unless one is working with sub-picosecond transmission lines, this glitch will probably never be noticed by most digital logic.

1. With an impedance discontinuity for such a short time period, it is difficult to accurately measure this effect. If it is difficult to measure this effect, should a design engineer worry about signal integrity issues for designs that operate below the mid-to-upper GHz range?

2. With the tolerance of production of the PCB at ± 10%, and the impedance discontinuity ± 20% for 15 ps, few components would notice this glitch, and in fact would absorb this discontinuity. Consequently, time domain analysis related to use of right-angle corners is not a concern for most PCB designs!

8.3.2 Frequency Domain Analysis

A question frequently asked is, How much radiated RF energy is really propagated from a right-angle corner? Research [2] shows that the magnitude of emissions is not as serious as was commonly assumed over the course of many years.

Various trace configurations were investigated. These configurations consist of a round corner, 45° and 90° angles with various trace widths. For

all test configurations, the amount of radiated emissions was negligible. The magnitude of emissions ranged from +2 to 5 dB. The accuracy of the test instrumentation is ± 4%.

Radiated emission from traces is attributed to the transmission line structure being an efficient radiator at λ/4 and λ/8, with signals being observed in the frequency range of 750 MHz and up. It is difficult to measure the magnitude of emissions from a trace corner when active logic devices are present. Numerous other areas within the PCB develop significantly greater amounts of energy than a trace corner, which is where we should focus our engineering effects. Also, stripline traces do not radiate; therefore, how could a stripline right-angle corner cause an EMI problem?

8.3.3 Summary of Effects from Right-Angle Corners

TIME DOMAIN (SIGNAL INTEGRITY CONCERNS). There are minor reflections from 90° or 45° corners. In theory, and by mathematical analysis, the impedance of a corner will decrease by a calculable amount. This impedance change is difficult to measure, even with very high bandwidth analyzers. The velocity of propagation of a signal within a transmission line (trace) is oblivious to the discontinuity unless one designs signals in the upper gigahertz frequency range or uses edge rates faster than 20 ps.

FREQUENCY DOMAIN. Radiated emissions exist. However, measurements up to 1 GHz do not show an increase for 90° or 45° corners that is significantly greater than the level of uncertainty of the measurement equipment. The average radiated emission from a right-angle corner is approximately +5 dB maximum. The discontinuities within component packages, connectors, layer jumping, vias, and common-mode currents within the transmission line will radiate at levels that far exceed any measurable effects from any corner configuration. Corners do not start to appear as radiated emissions until the upper MHz range (700 MHz and above), and even then, the magnitude of the emission is minimal. It is difficult, if not impossible, to measure radiated emissions from any trace corner configuration.

The main reason for not designing a PCB with right-angle corners lies with manufacturing. When traces are etched, the chemical etchant starts at the corner of trace. During etching, the corner will be etched back first by a certain amount, thus causing the physical dimensions to decrease. For a 20-mil trace, the amount of etch back is minimal. For a 5-mil trace, the finished etched trace may end up at 3 mils, which is a more serious problem than a wider trace. Functional problems may occur if a significant amount of current is transferred through the corner (fusing of the trace). In addition, delamination may occur. Delamination refers to the peeling of the trace from the board, thus destroying the trace during manufacturing and assembly.

Almost all CAD programs will allow prevention of routing traces at 90° angles. Do not turn off or disable this routing feature. Since clock signals must always be manually routed, it must be guaranteed that these traces are first routed without 90° angles prior to routing the rest of the board. When performing artwork cleanup for traces prior to release (usually called glossing the board), it should be guaranteed that all trace corners that were routed at 90° angles are converted to 45° angles or some other configuration for manufacturing reasons.

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Chapter 8 - Additional Design Techniques

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by Mark I. Montrose

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8.4 SELECTING FERRITE COMPONENTS

It is a well-known fact that ferrite devices (bead-on-lead, toroids, cores, split cores, wound beads, etc.) attenuate RF energy. The biggest difficulty in using a ferrite component is selecting the proper device for a specific application. Usually, the trial and error method is performed by the EMI or design engineer during attempts to solve a radiated or conducted emission problem. In reality, selection of a ferrite device is quite simple [5].

There are three common ways to select ferrites for suppression of unwanted signals, from least to most used for a particular application:

1. When used as a shield, the ferrite device isolates conductors, components, or circuits from stray electromagnetic fields.

2. When used with a capacitor, a low-pass filter is created that is inductive-capacitive at low frequencies and dissipative at higher frequencies.

3. Ferrite material prevents parasitic oscillations or attenuates unwanted signal coupling traveling along component leads, interconnecting wires, traces, or cables. When used as a lossy element, ferrite removes or absorbs electromagnetic energy present within a transmission line and dissipates this RF flux as heat.

For the last two applications, ferrite cores suppress EMI by eliminating or reducing high-frequency RF currents emanating from an EMI source. When a ferrite material is introduced, high-frequency impedance results, suppressing high-frequency RF currents. Theoretically, an ideal ferrite would provide high impedance at RF frequencies and zero impedance at all other frequencies. The impedance value is generally low, below 1 MHz. Depending on the ferrite material used, maximum impedance is usually observed between 10 MHz and 300 MHz.

The following are major applications for soft ferrite:

1. Low-level signals.

2. Power line filtering.

3. Suppression of RF energy.

Soft ferrite changes its magnetic state based on the environment in which the device is being used. Hard ferrite is a permanent polarization or magnetizing of a material, similar to a permamagnet with a north and south pole. Each application requires optimal intrinsic material characteristic selection and a required core geometry.

The selection of a particular ferrite material is based on the impedance the device presents to the circuit. Core material has magnetic losses that are represented by Eq. (8.5).

$$Z = R_s + j\omega L_s \tag{8.5}$$

Get MathML

where: Z = total impedance value of the ferrite material (ohms)

R_s	=	total series resistance, $R_m + R_e$ (ohms)
R_m	=	equivalent series resistance due to magnetic losses (ohms)
R_e	=	equivalent series resistance for copper losses (ohms)
L_s	=	inductive reactance (ohms)
ω	=	$2\pi f$
f	=	frequency (hertz)

The impedance of ferrite material is in reality a parallel combination of inductive reactance ($j\omega L_s$) and loss resistance (R_s), both of which are frequency dependent. The real component of the complex equation represents the loss portion, and the imaginary component represents the reactive.

At lower frequencies, the impedance is primarily lossy, which is a function of the material's permeability (μ). Most unwanted signals are thus reflected. At higher frequencies, inductive reactance increases, causing the total impedance to increase. Thus, unwanted signals are absorbed and dissipated as heat without affecting signal performance.

Examining the real component of the impedance equation, we observe that the permeability (μ) of different materials ranges from 10 to 15,000. This is principally due to the ferromagnetic resonance of the material. The higher the permeability, the lower the resonant frequency.

When selecting a ferrite material, consider the following:

- Frequency of the unwanted signal to be suppressed.
- Source of the energy (radiated or conducted).
- Environmental conditions. (Elevated temperatures will decrease overall impedance and performance.)
- Circuit impedance—source and load.
- Amount of attenuation required.
- Allowable space on the PCB.
- The impedance presented to the circuit by the ferrite material.
- The permeability value for optimal frequency range of operation.
- Alteration of the core size, shape, or length to change the impedance value.
- Bias (current flow through the material) will decrease the impedance to the point of nonfunctionality.
- Whether AC or DC current is passed through the device, excessive attenuation of a "wanted" signal could occur.
- Additional turns of wire will increase the impedance of shield beads or cores. (However, spectral bandwidth of performance is decreased.)

Different ferrite families, or material used in manufacturing the device, have different permeability values: inductive reactance and loss resistance. Commonly used materials and their range of filtering (based on permeability) are shown in Table 8.1.

Table 8.1: Frequency Range for Several Types of Ferrite Material

Open table as spreadsheet

Permeability	Frequencies Suppressed
2500μ	30 MHz or less

850µ	25 to 250 MHz
125µ	200 MHz and above

Custom materials with different permeability values are available from manufacturers for use at a particular frequency or range of frequencies. Generally, the higher the permeability, the lower the optimum attenuation frequency. Conversely, the lower the permeability, the higher the attenuation frequency. This is because low-frequency attenuation is reflective. High-frequency attenuation is limited by core size and circuit resonance.

In addition to selecting a material for a certain range of frequencies, consider attenuation desired for a particular application. Attenuation is calculated by Eq. (8.6), which is difficult to solve.

(8.6)
$$\text{Attenuation} = 20 \log_{10} \frac{(Z_s + Z_{sc} + Z_L)}{(Z_s + Z_L)}$$

Get MathML

where: Z_s = source impedance

Z_{sc} = suppressor core impedance

Z_L = load impedance

Equation 8.6 is dependent on the impedance of the source generating the noise and the impedance of the load receiving it. The result of this equation is in complex form.

Selection of a ferrite material cannot be based on permeability value alone. Consideration of core size, the environment, bias, and resistivity must also be taken into account.

The core size or shape determines the maximum impedance for a particular package size. Generally, as the length of the core increases, impedance increases versus the diameter for the same volume. To achieve greater impedance, select a core with a longer length, either circular, flat, or toroidal. Table 8.2 summarizes three different core sizes and the impedance presented to the circuit by the ferrite material.

Table 8.2: Comparison of Impedance from Common Ferrite Bead Materials

Open table as spreadsheet

Bead Type and Dimensions (L × OD × ID in mm)	Impedance (ohms)					
	1 MHz	5 MHz	10 MHz	20 MHz	30 MHz	50 MHz
µ = 850, 3.25 × 3.5 × 1.6	2	8	13	20	28	32
µ = 2500, 3.25 × 3.5 × 1.6	11	26	32	37	37	35
µ = 850, 7.5 × 7.65 × 2.25	5	18	29	40	58	61
µ = 2500, 7.5 × 7.65 × 2.25	25	47	58	61	61	60
µ = 850, 11.1 × 5.1 × 1.5	14	41	66	95	110	115
µ = 2500, 11.1 × 5.1 × 1.5	46	100	125	160	160	155

The environment also affects magnetic parameters, which change with temperature and field strengths. An increase in temperature will cause a decrease in overall impedance. For use at elevated temperatures, it is

important to select a ferrite material that decreases at a slower rate of change per degree C.

Bias refers to the amount of DC current passed through the core. An increase in bias will decrease the impedance more than any other environmental parameter. The magnetic field strength also causes significant degradation in impedance in the lower frequency ranges. To increase the DC-carrying capabilities of a ferrite device, a core shape with a built-in airgap should be selected. The larger the gap, the less effect bias will have on impedance. The higher the frequency, the less effect the gap and bias current will have on the device.

The resistivity of ferrite material varies depending on the value of the AC or DC current passed through the bead. This resistivity may cause excessive attenuation of a "wanted" signal, as if the ferrite bead was replaced by a resistor.

To increase the impedance of shield beads or cores, more turns of wire may be added. The impedance will increase in direct proportion to the turns squared. However, the frequency at which maximum impedance is reached is lowered due to the additional capacitive effects of the wire. The net effect of having wire winding on a core is to narrow the effective range of frequencies available for suppression of unwanted energy while increasing maximum impedance.

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Chapter 8 - Additional Design Techniques

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8.5 GROUNDED HEATSINKS

Grounded heatsinks, a new concept in suppression of RF energy within a PCB, finds use in specific applications and only for certain components. Grounded heatsinks are sometimes required when using VLSI processors operating in the 100-MHz range and above. These CPU and VLSI components require more extensive high-frequency decoupling and grounding than do most other parts of a PCB, especially if design techniques associated with the silicon die do not have slew rate control or other EMI mitigation features provided.

New technology in wafer fabrication easily allows component densities to exceed 1 million transistors per die. Consequently, some components consume 15 watts or more of DC power, and may far exceed 15 watts. These high-power devices require separate cooling provided by a fan built into a localized heatsink or by location of the processor adjacent to a remote fan. Since high-power, high-speed processors are being implemented in more designs, special design techniques are now required for both EMI suppression and heat removal at the component level.

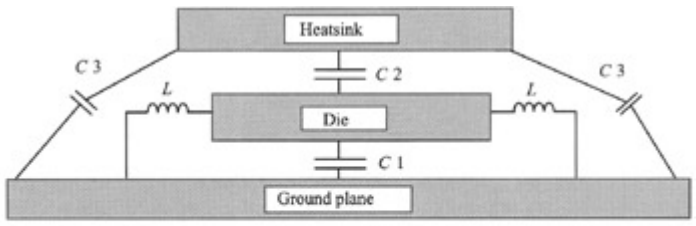
When we examine the function of a heatsink in the thermodynamic domain, removal of heat developed internal to the processor must occur. Components that dissipate large amounts of heat are usually encapsulated in a ceramic case, since ceramic packaging will dissipate more heat than a plastic package. Ceramic cases also cost more. Certain components, owing to large junction temperatures between internal gates, generate more heat than the ceramic package can dissipate; hence, a heatsink is required for thermal cooling.

The speed of a processor is directly related to the density of the internal circuitry. Power dissipation per square area is also increased. Semiconductor devices have a limited thermal range of operation. The surface area of the processor must be increased by placing a heatsink in contact with the processor. Airflow, provided by fans, is limited to the volume of air passing over the surface of the heatsink. Fans are also sometimes limited to the amount of airflow they can provide for acoustic reasons. To increase heat dissipation, large heatsinks are required.

Heatsinks are usually made of metal and contain fin structures. Depending on processor harmonics, heatsink dimensions can become electrically able to start radiating RF energy. Because of the close proximity of the processor, related to other circuits and subassemblies, RF noise may be coupled through various paths, for example, internal cables or apertures, both of which can leak to the outside environment.

Having briefly discussed the function of heatsinks in the thermodynamic domain, we now examine a metal heatsink in the RF domain. For proper thermal implementation and use of heatsinks, a thermal conductor (silicon compound or mica insulation) is provided. If the heatsink is not very heavy, it is common to use thermally conductive, but electrically nonconductive adhesive. This conductor contains excellent thermal properties for transferring heat from the component to the heatsink. Glue is usually not strong enough to stand rigorous shock and vibration tests. Larger heatsinks are either bolted onto the metal lid or screw secured to the PCB.

Having examined the thermal need for heatsinks, we observe the following characteristics (Figs. 8.9 and 8.10):



L = package lead inductance
C1 = distributed capacitance from the die to the ground plane
C2 = distributed capacitance from the heatsink to the die
C3 = distributed capacitance from heatsink to ground plane or chassis

Typical self-resonant frequency of VLSI processors is approximately 200–800 MHz with heatsink.

Figure 8.9: Grounded heatsink theory of operation.

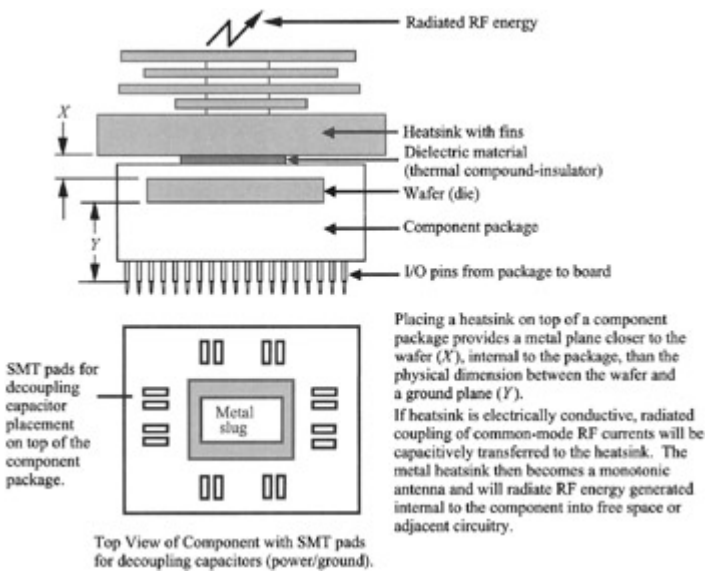

Radiated RF energy
X
Heatsink with fins
Dielectric material
(thermal compound-insulator)
Wafer (die)
Component package
Y
I/O pins from package to board
SMT pads for decoupling capacitor placement on top of the component package.
Metal slug
Top View of Component with SMT pads for decoupling capacitors (power/ground).
Placing a heatsink on top of a component package provides a metal plane closer to the wafer (X), internal to the package, than the physical dimension between the wafer and a ground plane (Y).
If heatsink is electrically conductive, radiated coupling of common-mode RF currents will be capacitively transferred to the heatsink. The metal heatsink then becomes a monotonic antenna and will radiate RF energy generated internal to the component into free space or adjacent circuitry.

Figure 8.10: Grounded heatsink implementation.

- The wafer dies operating at high clock speeds, generally 100 MHz and above, generate large amounts of common-mode RF current internal to the device package.
- Decoupling capacitors remove *differential-mode* RF current that exists only between the power and ground system.
- Certain ceramic packages contain solder pads on top of the package case to provide additional differential-mode decoupling. Decoupling capacitors minimize ground bounce and board-level-induced noise voltage created by the simultaneous switching of all component pins under maximum capacitive load.
- The wafer (or die) internal to the package (Fig. 8.10) is located closer to the top of the case (dimension *X*) than the bottom of the package (dimension *Y*). Therefore, height separation from the silicon die to an image plane internal to the PCB is greater than the distance of the die to the top of the package case and heatsink. *Common-mode* RF currents generated internally within the wafer have no place to couple to 0V-reference. Hence, RF energy is radiated from the device into free space. *Differential-mode* decoupling capacitors will not remove *common-mode* noise created within the component.
- Placing a metal heatsink on top of the component provides a 0V-reference (image plane) closer to the wafer than the image plane on the PCB. Tighter *common-mode* RF coupling thus occurs between the die and heatsink rather than between the die and the first reference plane of the PCB.
- Common-mode coupling that occurs to the heatsink now causes this thermodynamically required part to become a *monotonic antenna*, perfect for radiating RF energy into free space.

A processor can be an effective radiating source of RF energy. Adding a metal heatsink means more design requirements must be considered, and not just for thermodynamic concerns. In general, as the size of the heatsink increases, radiation efficiency also increases. The maximum amount of radiation will occur at different frequencies, depending on the geometry of the heatsink and the self-resonant frequency of the assembly, if the heatsink is a metallic structure.

The net result of using a metal heatsink is the same as placing a monotonic antenna inside the product to radiate clock harmonics and internally generated RF spectral energy throughout the entire frequency

spectrum. To de-energize this antenna, the heatsink must be grounded. Although this concept is very simple, it is virtually ignored within the field of PCB design and layout for RF energy suppression.

Heatsinks must be bonded to the ground planes (or 0V-reference) of the PCB by a metallic connection. Use of a fence (similar to a vertical bus bar) from the PCB to the heatsink will encapsulate the processor. This fence allows for a Faraday shield to be present around the processor, thus preventing common-mode noise RF energy developed internal to the package from radiating into free space or coupling onto nearby components, cables, and peripherals or into aperture slots. A technique for providing grounding for the heatsink is shown in Fig. 8.11.

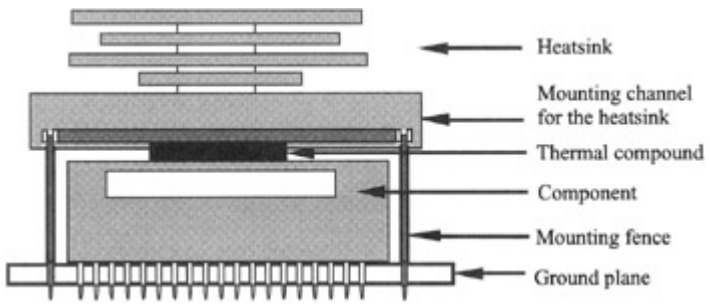


Figure 8.11: Grounding the heatsink.

When a metal lid or slug on the component (if provided) is connected directly to the heatsink, there exists a finite amount of package inductance between the two ground assemblies. These two grounds, being at different potentials, develop common-mode RF energy between the two. If the component is further linked to the metal heatsink by means of vias and epoxy, this connection will push the heatsink to a slightly different potential than the device's ground reference, thus exacerbating development of common-mode energy.

Reduced Instruction Set Computing (RISC) processors or VLSI components generally have a high, internal self-resonant frequency that is a combination of the manufacturing process and the internal clock speed. This self-resonant frequency is in addition to the overall impedance present in the power and ground plane structure. Consequently, VLSI processors radiate RF energy more than many other components, if RF suppression is not incorporated by the component manufacturer in the silicon die. Any attempt to remove this internally generated self-resonant RF frequency, using standard suppression techniques, is almost impossible except through use of the heatsink as a *common-mode decoupling capacitor*.

This heatsink is generally used in conjunction with differential-mode decoupling capacitors located on the top of the components' ceramic package, if provisions are available for top-mounted capacitors. These top-mounted capacitors are in addition to standard, differential-mode (decoupling) capacitors located directly on the PCB. A *differential-mode* decoupling capacitor connects directly between the power and ground planes to remove switching noise injected into these planes during a logic transition state. A *common-mode* decoupling capacitor provides an AC shunt to couple common-mode noise generated internally from the die of the wafer into the 0V-reference system.

A grounded heatsink must be at *ground potential*, whereas the active component is at *RF voltage potential*. The thermal compound is a dielectric insulator between two large parallel plates. The definition of a capacitor is fulfilled. Thus, a grounded heatsink works as one large *common-mode decoupling capacitor* (component and ground). This common-mode capacitor AC couples or shunts RF energy away from the device. Optional discrete capacitors located on top of the device package, or directly on the PCB, are used for *differential-mode* decoupling (power and ground). A common-mode capacitor has completely different functions than typical differential-mode capacitors.

Using a grounded heatsink creates

1. A thermal device to remove heat generated internal to the package.
2. A Faraday shield preventing RF energy from frequency-generating (clock) circuitry, internal to the processor, from radiating into free space or corrupting adjacent components.
3. A *common-mode* decoupling capacitor that removes common-mode

RF currents directly from the die, inside the package, by AC coupling RF energy from die to ground.

If a grounded heatsink is implemented, the grounding posts of the fence (spring fingers or other PCB mounting method employed) must connect to the 0V-reference in the PCB on at least 1/4 in. (6.4 mm) centers around the processor. At each and every ground connection, two sets of parallel decoupling capacitors should be installed, alternating between each ground pin of the fence, with 0.1 µF in parallel with 0.001 µF, and 0.01 µF in parallel with 100 pF. RF spectral distribution from RISC processors and similar components generally exceed 1-GHz bandwidth. RISC or VLSI components also require more extensive multipoint grounding around all four sides of the device package than most other types of processors. These decoupling capacitor values complement the approximate $\lambda/4$ mechanical size of typical heatsinks, making them efficient suppressors of EMI spectral energy.

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Chapter 8 - Additional Design Techniques

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8.6 LITHIUM BATTERY CIRCUITS

International safety agencies require protection against explosion from lithium batteries should an abnormal fault occur, such as a short circuit or reverse bias during a charging cycle. Lithium battery circuits may consist of a discrete battery with passive components, or may be included as part of a NVRAM (Non-Volatile RAM) or Non-Volatile Clock Calendar module. The battery must be provided with reverse current protection. This protection must be redundant in nature and typically consists of two diodes back to back or a diode and a resistor in series. A typical lithium battery circuit with common protection components is shown in Figure 8.12.

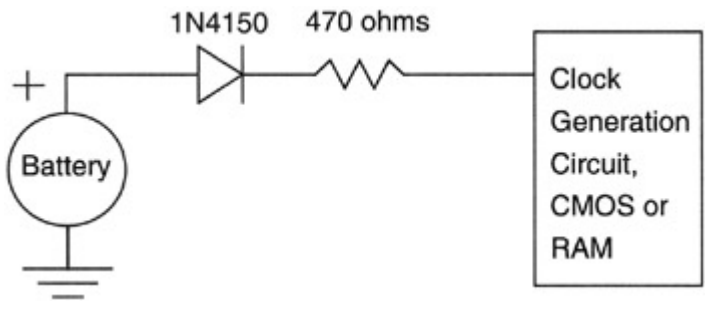

Figure 8.12: Lithium battery protection design requirement.

The reason for two components is redundancy. If one component should fail, a second device remains, thus protecting the circuitry, people, or domestic animals from injury if a single fault condition occurs. Product safety requirements mandate the performance of abnormal tests on circuits considered hazardous. To successfully pass these tests, two levels of protection are thus required.

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8.7 BNC CONNECTORS

BNC connectors require special considerations when incorporated on a PCB. For interconnects where the braid of the coax is required for RF shielding, ground the shell of the connector to chassis ground at the bulkhead, or I/O panel through a low-impedance path to 0V-reference. It should be verified that this ground connection is to chassis ground and *not* to the isolated or digital ground section.

For applications where the shell of the BNC connector is *signal return* and is not used as a *RF return shield*, the shell of the BNC connector, must be connected through a low-impedance path to the 0V-reference of the signal return circuit. *Do not* connect the ground (outer barrel) pin of the BNC connector to the I/O isolated (quiet ground) area. In addition, *do not* connect the shell of the BNC connector to the chassis ground (I/O bracket). To implement this unique scheme, an isolated BNC connector available from many vendors must be used. These connectors guarantee that the shell and internal signal pin of the connector are isolated from chassis ground. This scheme *will* cause problems if not properly implemented (Fig. 8.13).

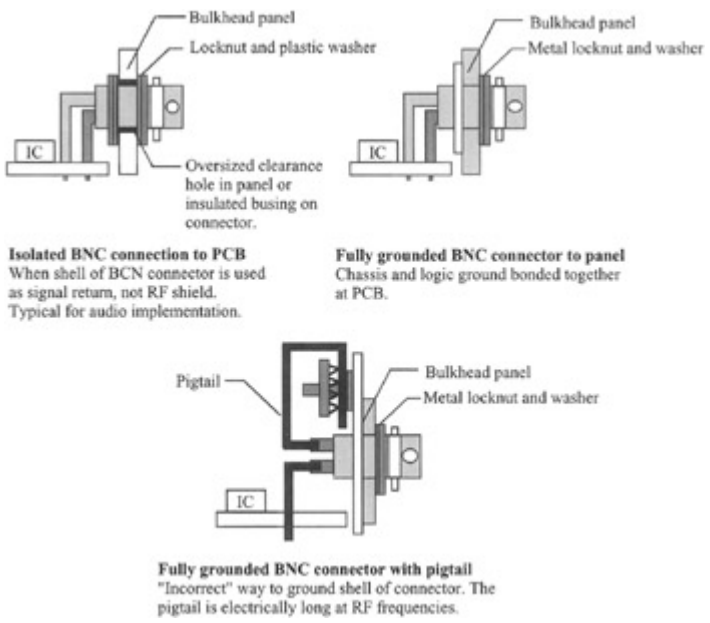
Bulkhead panel
Locknut and plastic washer
IC
Oversized clearance hole in panel or insulated busing on connector.
Isolated BNC connection to PCB
When shell of BCN connector is used as signal return, not RF shield.
Typical for audio implementation.
Bulkhead panel
Metal locknut and washer
IC
Fully grounded BNC connector to panel
Chassis and logic ground bonded together at PCB.
Pigtail
Bulkhead panel
Metal locknut and washer
IC
Fully grounded BNC connector with pigtail
"Incorrect" way to ground shell of connector. The pigtail is electrically long at RF frequencies.

Figure 8.13: BNC connector configurations.

Pigtails must never be used, under any condition, to connect the shell of the BNC connector to chassis ground or to any other ground system. Measurements are well documented showing a 40- to 50-dB difference between a pigtail and a 360° connection of the cable shield to the BNC connector shell in the 15- to 200-MHz frequency range related to RF emission. In addition to improvement in reducing RF emissions, a greater level of ESD immunity is provided due to less lead inductance presented to the ESD event. For most applications, the recommendation for cable shields is to connect the cable shield to the BNC connector shell in a 360° fashion. This backshell then mates with a bulkhead panel containing a solid metallic contact with chassis ground.

A concern that mandates mandatory grounding of BNC connectors lies with product safety requirements related to secondary short-circuit tests. If a fault condition develops on an interconnect, the coaxial cable can assume a voltage potential. These voltage potentials can than cause an electric shock hazard. If the shell of the connector is bonded to chassis ground, fault currents that may be present on the braid of the coax must be

safety shunted to earth ground. This earth ground, if bonded to the chassis ground (providing one exists), will present this fault circuit from causing harm. This protection is valid only when a third wire AC mains safety ground is present within the product's power cord and mains receptacle.

Excellent reference books discuss techniques for I/O interconnects using a large number of connector families and types. Many of these books are listed in the References and Bibliography section.

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8.8 CREEPAGE AND CLEARANCE DISTANCES

Another concern with safety agencies lies with the potential risk of electric shock that may occur between traces and conductive parts of a system. Although creepage and clearance are not directly associated with EMI, a discussion of this topic must be presented in a book for PCB designers, since all products must comply with *both* safety and EMC requirements. One cannot design a product to be compliant for only EMC. Both safety and EMC must be considered simultaneously during the design and layout cycle.

Creepage and clearance, defined by harmonized safety standards, are described in the following list and illustrated in Fig. 8.14 [7]:

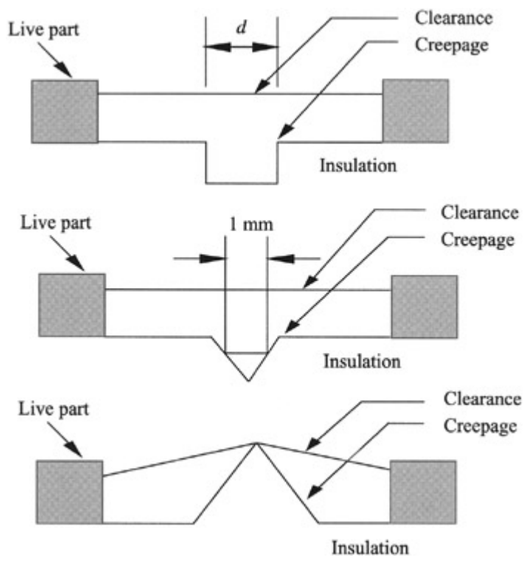

Figure 8.14: Creepage and clearance distance definition.

- Creepage is the shortest path between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured along the surface of the insulation.
- Clearance is the shortest distance between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured through air.
- Bounding surface is the outer surface of the electrical enclosure considered as though metal foil was pressed into contact with the accessible surface of insulation material.

The creepage and clearance distance must be maintained primarily because high-voltage circuits on a PCB may be subjected to a failure condition. Failures include electrical shorts between primary-to-secondary, primary-to-ground, or primary-to-primary circuits. To prevent a shock hazard resulting from an unexpected fault, the designer must route specific traces with a certain amount of spacing (distance) between high-energy (voltage) sources and secondary or ground circuits. This requirement is especially critical in power supplies and telecommunication products.

Under high-voltage or fault conditions, arcing may occur across the conformal coating, the soldermask, or between traces and a bounding surface. Consequently, a high level of voltage and current may be present that creates a situation for risk of fire or electric shock. International safety standards specify minimum creepage and clearance distances for various types of equipment under specific operating conditions identified as pollution degrees. Tables 8.3 to 8.6 present details on distance requirements for both creepage and clearance, extracted from internationally harmonized safety standards for information technology equipment. These distances are recognized worldwide and are strictly enforced. The values in the tables are the minimum values that shall be applied, after taking into account manufacturing tolerances and deformation. These variations occur as a result of handling, shock, and vibration encountered during manufacture, transport, and normal use. For all power systems, the main supply voltage in Tables 8.3, 8.4, 8.5 and 8.6 is the phase-to-neutral voltage.

Table 8.3: Clearance Distances for Primary Current Carrying Traces

Open table as spreadsheet

Minimum clearances for insulation in primary circuits, and between primary and secondary circuits mm																
Insulation working voltage (see 2.2.7) up to and Including		Circuits subject to Installation category II														
		Nominal mains supply voltage ⩽ 150 V (Translent rating 1500 V)						Nominal mains supply voltage >150 V ⩽ 300 V (Translent rating 2500 V)						Nominal mains supply voltage > 300 V ⩽ 600 V (Translent rating 4000 V)		
V peak or d.c. V	V r.m.s. (sinusoidal) V	Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1, 2 and 3		
		Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R
71	50	0.4	1.0 (0.7)	2.0 (1.4)	1.0	1.3 (1.0)	2.6 (2.0)	1.0	2.0 (1.7)	4.0 (3.4)	1.3	2.0 (1.7)	4.0 (3.4)	2.0	3.2 (3.0)	6.4 (6.0)
210	150	0.7	1.0 (0.7)	2.0 (1.4)	1.0	1.3 (1.0)	2.6 (2.0)	1.4	2.0 (1.7)	4.0 (3.4)	1.7	2.0 (1.7)	4.0 (3.4)	2.0	3.2 (3.0)	6.4 (6.0)
420	300	Op 1.7 B/S 2.0 (1.7) R 4.0 (3.4)												2.5	3.2 (3.0)	6.4 (6.0)
840	600	Op 3.0 B/S 3.2 (3.0) R 6.4 (6.0)														
1,400	1,000	Op/B/S 4.2 R 6.4														
2,800	2,000	Op/B/S/R 8.4														
7,000	5,000	Op/B/S/R 17.5														
9,800	7,000	Op/B/S/R 25														
14,000	10,000	Op/B/S/R 37														
28,000	20,000	Op/B/S/R 80														
42,000	30,000	Op/B/S/R 130														

Table 8.4: Additional Clearance Distances for Use with High- Voltage Applications

Open table as spreadsheet

Additional clearances for insulation in primary circuits with repetitive peak voltages exceeding the peak value of the mains supply voltage							
Nominal mains supply voltage ⩽ 150 V				Nominal mains supply voltage > 150 V ⩽ 300 V		Additional clearance mm	
Pollution degrees 1 and 2		Pollution degree 3		Pollution degrees 1, 2 and 3		Operational, basic or supplementary Insulation	Reinforced Insulation
Maximum repetitive peak voltage V		Maximum repetitive peak voltage V		Maximum repetitive peak voltage V			
210	(210)	210	(210)	420	(420)	0	0
298	(290)	294	(300)	493	(497)	0.1	0.2
386	(370)	379	(390)	567	(574)	0.2	0.4
474	(450)	463	(480)	640	(651)	0.3	0.6
562	(530)	547	(570)	713	(728)	0.4	0.8
650	(610)	632	(660)	787	(805)	0.5	1.0

738	(690)	716	(750)	860	(881)	0.6	1.2
826	(770)	800	(840)	933	(958)	0.7	1.4
914	(850)	-	-	1,006	(1,035)	0.8	1.6
1,002	(930)	-	-	1,080	(1,112)	0.9	1.8
1,090	(1,010)	-	-	1,153	(1,189)	1.0	2.0
-	-	-	-	1,226	(1,266)	1.1	2.2
-	-	-	-	1,300	(1,343)	1.2	2.4
-	-	-	-	-	(1,420)	1.3	2.6

Table 8.5: Clearance Distance Chart for Secondary Circuits

➡ Open table as spreadsheet

Minimum clearances in secondary circuits mm																		
Insulation working voltage up to and Including		Circuits subject to Installation Category I (see condition 5)																
		Nominal mains supply voltage ⩽ 150 V (Translent rating of secondary circuit 800 V)						Nominal mains supply voltage 150 V ⩽ 300 V (Translent rating of secondary circuit 1 500 V)						Nominal mains supply voltage > 300 V ⩽ 600 V (Translent rating of secondary circuit 2 500 V)			Circuits not subjected to transient overvoltage (see condition 4)		
V peak or d.c. V	V r.m.s. (sinusoldal)	Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1, 2 and 3			Pollution degrees 1 and 2 only		
		Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R
71	50	0.4	0.7 (0.4)	1.4 (0.8)	1.0	1.3 (1.0)	2.6 (2.0)	0.7	1.0 (0.7)	2.0 (1.4)	1.0	1.3 (1.0)	2.6 (2.0)	1.7	2.0 (1.7)	4.0 (3.4)	0.4	0.4	0.8
140	100	0.6	0.7 (0.6)	1.4 (1.2)	1.0	1.3 (1.0)	2.6 (2.0)	0.7	1.0 (0.7)	2.0 (1.4)	1.0	1.3 (1.0)	2.6 (2.0)	1.7	2.0 (1.7)	4.0 (3.4)	0.6	0.7 (0.6)	1.4 (1.2)
210	150	0.6	0.9 (0.6)	1.8 (1.2)	1.0	1.3 (1.0)	2.6 (2.0)	0.7	1.0 (0.7)	2.0 (1.4)	1.0	1.3 (1.0)	2.6 (2.0)	1.7	2.0 (1.7)	4.0 (3.4)	0.6	0.7 (0.6)	1.4 (1.2)
280	200	Op 1.1 B/S 1.4 (1.1) R 2.8 (2.2)												1.7	(2.0) (1.7)	4.0 (3.4)	1.1	1.1	2.2
420	300	Op 1.6 B/S 1.9 (1.6) R 3.8 (3.2)												1.7	2.0 (1.7)	4.0 (3.4)	1.4	1.4	2.8
700	500	Op/B/S 2.5 R 5.0																	
840	600	Op/B/S 3.2 R 5.0																	
1,400	1,000	Op/B/S 4.2 R 5.0																	
2,800	2,000	Op/B/S/R 8.4																	
7,000	5,000	Op/B/S/R 17.5																	
9,800	7,000	Op/B/S/R 25																	
14,000	10,000	Op/B/S/R 37																	
28,000	20,000	Op/B/S/R 80																	
42,000	30,000	Op/B/S/R 130																	

Table 8.6: Creepage Distances Requirements

➡ Open table as spreadsheet

Minimum creepage distances mm							
Working voltage up to and Including V r.m.s. or d.c.	OPERATIONAL, BASIC and SUPPLEMENTARY INSULATION						
	Pollution degree 1	Pollution degree 2			Pollution degree 3		
	Material group	Material group			Material group		
	I, II, IIIa + IIIb	I	II	IIIa + IIIb	I	II	IIIa + IIIb
50	Use the appropriate CLEARANCE from table 3 or table 5	0.6	0.9	1.2	1.5	1.7	1.9
100		0.7	1.0	1.4	1.8	2.0	2.2
125		0.8	1.1	1.5	1.9	2.1	2.4
150		0.8	1.1	1.6	2.0	2.2	2.5
200		1.0	1.4	2.0	2.5	2.8	3.2
250		1.3	1.8	2.5	3.2	3.6	4.0
300		1.6	2.2	3.2	4.0	4.5	5.0
400		2.0	2.8	4.0	5.0	5.6	6.3
600		3.2	4.5	6.3	8.0	9.6	10.0
1,000		5.0	7.1	10.0	12.5	14.0	16.0

Within the tables, the following terms and references are used:

Insulation Definition

- *Operational Insulation:* Insulation needed for the correct operation of the equipment.

  Note By definition operational insulation does not protect against electric shock. It may, however serve to minimize exposure to ignition and fire. The use of air as a barrier between a conductive part and dead metal is considered operational insulation.

- *Basic Insulation:* Insulation to provide basic protection against electric shock. This insulation may be a PVC jacket over wire or shrink tubing over quick disconnect terminals.

- *Supplementary Insulation:* Independent insulation applied in addition to *Basic Insulation* in order to ensure protection against electric shock in the event of a failure of the *Basic Insulation*.

- *Double Insulation:* Insulation comprising both *Basic Insulation* and *Supplementary Insulation*.

- *Reinforced Insulation:* A single insulation system that provides a degree of protection against electric shock equivalent to *Double Insulation* under the conditions specified in the standard.

  Note The term "insulation system" does not imply that the insulation has to be in one homogeneous piece. It may comprise several layers that cannot be tested as *Supplementary* or *Basic Insulation*.

- *Working Voltage:* The highest voltage to which the insulation under consideration is, or can be, subjected when the equipment is operating at its *Rated Voltage* under conditions of normal use.

Definition of Pollution Degrees

- Pollution Degree 1: Applicable to components and assemblies that are sealed to exclude dust and moisture.

- Pollution Degree 2: Generally applicable to equipment covered by the scope of the standard (applies to most equipment).

- Pollution Degree 3: Applicable where a local internal environment within the equipment is subject to conductive pollution or to dry nonconductive pollution which could become conductive due to expected condensation.

Chapter 8 - Additional Design Techniques

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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8.9 CURRENT-CARRYING CAPACITY OF COPPER TRACES

The power-handling capability of copper traces is based on cross-sectional area and is related to temperature rise. For a specific cross-sectional area, the temperature rise within a trace, above ambient levels, is approximately proportional to the power dissipated in the trace. An excessively large temperature rise makes circuits unreliable, heats up the dielectric material, and may cause destruction of the trace. To be conservative during the design cycle, an upper limit on the heating of traces should not exceed 10°C above ambient.

Figure 8.15 illustrates the current-carrying capability of traces, based on the amperage applied and cross-sectional area for a specific weight of copper [8, 9].

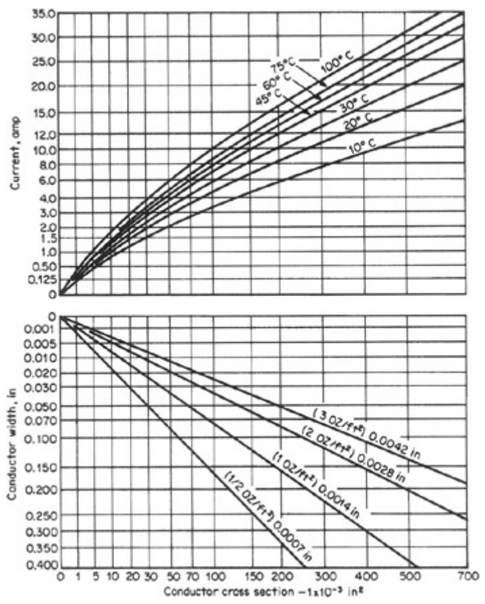

Figure 8.15: Current-carrying capacity of copper traces.

To illustrate how to read these charts, assume a 0.010-in. trace is constructed of 1-oz copper. The current-carrying capacity at 20°C is 1.2A. Locate the conductor width (bottom chart, vertical axis) and travel across to the appropriate weight of the copper, in this case, 1 oz. Draw a straight line up to the upper chart and stop at the desired temperature of operation. Read maximum current value on the vertical axis of the upper chart.

The curves include a nominal 10% derating (on a current basis) to allow for normal variation in etching techniques, copper thickness, conductor width estimates, and cross-sectional area. An additional derating of 15% (current-wise) is suggested under the following conditions:

1. For panel thickness of 0.031 in. (0.8 mm) or less.

2. For conductor thickness of 3 oz (108 µm) or thicker.

High-power, high-current-carrying traces pose a serious constraint except for large power distribution buses, networks, or planes. As thin-film technology is being used on a frequent basis, heating limitations become a serious design concern.

The temperature of a trace, or wire, depends on the environment within which the transmission line operates, and on whether the wire is insulated, coiled, or straight. Since resistance is distributed over the length of the trace, this parameter plays a part in the temperature rise equation. Heating is proportional to the square of the current. Temperature rise is exponentially related to the duration of current flow.

As the temperature level increases under heavy current loads, so does the resistance. This temperature rise serves to reduce the current present, if the source is voltage. If the source is current, resistance increases with power dissipation per the equation $P = I^2R$.

The approximate fusing current of a wire, *not* a PCB trace, is given in Eq. (8.7) [10].

$$I = \sqrt[3]{K * d} \tag{8.7}$$

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where K = a constant that depends on metal composition
d = wire diameter (inches)

To illustrate this equation for an 18 AWG copper wire, d = 0.0403 in. and K = 10,244 (copper, the most common material used in PCB trace construction).[1]

$$I = \sqrt[3]{10{,}244 * 0.043}$$

$$I = 82.9 \text{ Amperes}$$

Get MathML

The melting temperature for hard-drawn copper wire is 1981 °F or 1083°C.

Traces that are used in fusing applications are specified in terms of power ($I^2 * \Delta T$). Curves are published in various application notes from fuse manufacturers. Given the same conditions, one could publish $I^2 * \Delta T$ curves for various sizes of copper wires and PCB traces.

Since the melting temperature of copper is extremely high, one can largely ignore ambient temperature (e.g., the ΔT in the equation).

Table 8.7 presents a conversion chart for PCB finished trace widths related to standard wire gauges. The numbers in this table are to be used for the d parameter of Eq. (8.7).

Table 8.7: Conversion Chart for PCB Finished Trace Widths Related to Standard Wire Gauges

Open table as spreadsheet

					NON-PLATED WIDTH (inches)			PLATED WIDTH (inches)			RESISTANCE/INCH		
AWG	Diameter (inches)	Diameter (mm)	Area in^2	Area mm^2	½ OZ. (0.00068″)	1 OZ. (9.00135″)	2 OZ. (0.00270″)	½ OZ. (0.00168″)	1 OZ. (0.00235″)	2 OZ. (0.00370″)	mΩ 20°C	mΩ 50°C	mΩ 75°C
39	0.003531	0.089687	0.000010	0.006318	0.014400	0.007254	-	0.005829	-	-	69.317584	77.427742	84.186206
38	0.003965	0.100711	0.000012	0.007966	0.018158	0.009146	-	0.007350	-	-	54.973384	61.405270	66.765175
37	0.004453	0.113106	0.000016	0.010048	0.022903	0.011536	-	0.009270	-	-	43.584640	48.684043	52.933545
36	0.005000	0.127000	0.000020	0.012668	0.028875	0.014544	-	0.011687	-	-	34.569957	38.614642	41.985213
35	0.005615	0.142621	0.000025	0.015976	0.036415	0.018342	0.009171	0.014739	0.010537	-	27.411912	30.619106	33.291767
34	0.006305	0.160147	0.000031	0.020143	0.045915	0.023127	0.011564	0.018584	0.013286	-	21.740457	24.284091	26.403785
33	0.007080	0.179832	0.000039	0.025399	0.057896	0.029162	0.014581	0.023434	0.016753	-	17.241392	19.258635	20.939671
32	0.007950	0.201930	0.000050	0.032025	0.072999	0.036770	0.018385	0.029547	0.021123	0.013416	13.674284	15.274175	16.607418
31	0.008928	0.226771	0.000063	0.040389	0.092064	0.046373	0.023186	0.037264	0.026640	0.016920	10.842526	12.111102	13.168248
30	0.010030	0.254762	0.000079	0.050975	0.116194	0.058527	0.029264	0.047031	0.033622	0.021355	8.5900867	9.595998	10.433608
29	0.011260	0.286004	0.000100	0.064244	0.146439	0.073762	0.036881	0.059273	0.042374	0.026913	6.816510	7.614042	8.2786512
28	0.012640	0.321056	0.000125	0.080956	0.184533	0.092950	0.046475	0.074692	0.053397	0.033914	5.409345	6.042239	6.569650

27	0.014200	0.360680	0.000158	0.102172	0.232894	0.117309	0.058655	0.094266	0.067391	0.042802	4.286099	4.787572	5.205467
26	0.015940	0.404876	0.000200	0.128746	0.293466	0.147820	0.073910	0.118784	0.084918	0.053934	3.401435	3.799403	4.131043
25	0.017900	0.454660	0.000252	0.162354	0.370073	0.186407	0.093203	0.149791	0.107085	0.068013	2.697322	3.012909	3.275898
24	0.020100	0.510540	0.000317	0.204715	0.466630	0.235043	0.117522	0.188874	0.135025	0.085759	2.139177	2.389461	2.598031
23	0.022570	0.573278	0.000400	0.258119	0.588361	0.296360	0.148180	0.238146	0.170249	0.108131	1.696585	1.895086	2.060503
22	0.025350	0.643890	0.000505	0.325622	0.742227	0.373863	0.186931	0.300425	0.214772	0.136409	1.344878	1.502229	1.633354
21	0.028450	0.722630	0.000636	0.410130	0.934858	0.470891	0.235446	0.378395	0.270512	0.171812	1.067762	1.192690	1.296797
20	0.031960	0.811784	0.000802	0.517572	1.179762	0.594251	0.297125	0.477523	0.341378	0.216821	0.846107	0.945102	1.027597
19	0.035890	0.911606	0.001012	0.652686	1.487743	0.749382	0.374691	0.602182	0.430496	0.273423	0.670953	0.749454	0.814872
18	0.040300	1.023620	0.001276	0.822939	1.875820	0.944857	0.472429	0.759260	0.542790	0.344745	0.532143	0.594404	0.646288
17	0.044710	1.135634	0.001570	1.012900	2.308821	1.162962	0.581481	0.934523	0.668084	0.424324	0.432344	0.482928	0.525082
16	0.049120	1.247648	0.001895	1.222571	2.786748	1.403695	0.701848	1.127969	0.806378	0.512159	0.358197	0.400106	0.435030
15	0.053530	1.359662	0.002251	1.451950	3.309600	1.667058	0.833529	1.339600	0.957671	0.608251	0.301609	0.336897	0.366304
14	0.057940	1.471676	0.002637	1.701039	3.877376	1.953049	0.976524	1.569414	1.121964	0.712599	0.257443	0.287564	0.312665
13	0.062350	1.583690	0.003053	1.969837	4.490073	2.261669	1.130834	1.817413	1.299257	0.825204	0.222314	0.248324	0.270000
12	0.066760	1.695704	0.003500	2.258343	5.147705	2.592918	1.296459	2.083595	1.489549	0.946065	0.193913	0.216600	0.235507
11	0.071170	1.807718	0.003978	2.566559	5.850256	2.946796	1.473398	2.367961	1.692840	1.075182	0.170626	0.190589	0.207225

[1]Equation and variables extracted from *Reference Data for Engineers*, 6th ed., ITT, July 1981, Table 39, pp. 4–54.

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Chapter 8 - Additional Design Techniques

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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8.10 FILM

Because of the increasing density, the manufacturing process needs to be monitored closely. Of special concern are test coupons, layer stackup window, stacking stripes, and test points.

TEST COUPONS. Test coupons contain dummy traces that are routed on an external, disposable part of the PCB. One test trace is provided per routing layer. Test traces allow for easy measurement of the actual impedance of the signal planes. These dummy traces validate the quality control process of fabrication by the board vendor, assuring that the assembly was manufactured within specified requirements. Test traces and their pads are usually found on breakaway islands, not on the main artwork or final assembly. For backplanes and PCBs with high-speed circuits, test traces should be placed directly within the artwork, if not part of the design.

LAYER STACKUP WINDOW. Etched onto each layer of the PCB is a number, in a box, that reflects the identity of a layer internal to the board stackup. The advantage of using a layer stackup window is to help identify how many layers physically exist. If experimentation on routing layers and image planes occurs for performance optimization, during debug and EMI evaluation, this stackup window may assist in identifying different board stackup schemes and the number of layers used.

STACKING STRIPES. Stacking stripes is a technique by which copper from all layers is routed to the outside edge of the board. This copper is nonfunctional and can be viewed when looking at the side of the board. Each stripe is longer than its neighbor, followed by a single strip of a specific trace width. Use of a small handheld microscope will allow determination of the various layers (power, ground, or signal), plus final etched trace width. An inexpensive microscope can be purchased with a graduated scale for accurate measurement of finished trace width. An example of stacking stripes is given in Fig. 8.16.

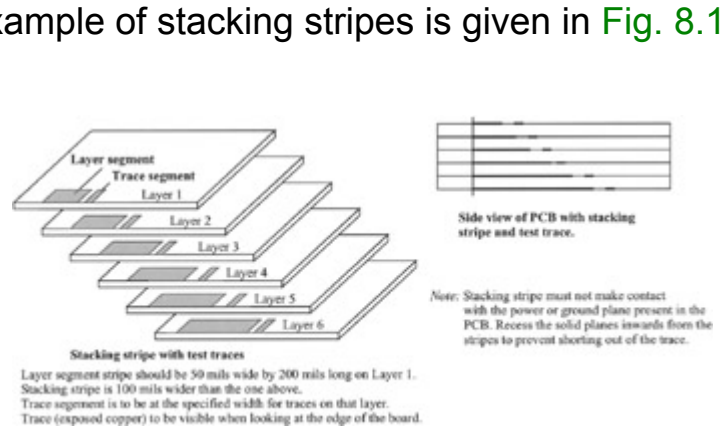
Layer segment
Trace segment
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Stacking stripe with test traces
Layer segment stripe should be 50 mils wide by 200 mils long on Layer 1.
Stacking stripe is 100 mils wider than the one above.
Trace segment is to be at the specified width for traces on that layer.
Trace (exposed copper) to be visible when looking at the edge of the board.
Side view of PCB with stacking stripe and test trace.
Note: Stacking stripe must not make contact with the power or ground plane present in the PCB. Recess the solid planes inwards from the stripes to prevent shorting out of the trace.

Figure 8.16: Stacking stripes and trace width description.

TEST POINTS. Test points are used to assist in analyzing whether a broken trace or a faulty component exists within the manufactured product. They allow for ease of debugging a bare board prior to being assembled with components.

Prior to specification of physical dimension (spacing between layers, trace width, and the like), a PCB manufacturer should be consulted for optimal design parameters and details on how the board is to be manufactured. Manufacturing details are generally not well known or understood by design engineers. Board vendors can provide information on base material, prepreg, actual dielectric value, trace width dimensions (for impedance control), height of a signal layer to a reference plane, and the like.

Core and prepreg refer to material composition. *Core* is the substrate that contains a thin sheet of copper laminated on both sides, whereas *prepreg* is glue material (epoxy resin based) placed between cores and heated, which secures various layers together. The thickness of the prepreg determines the spacing between the core layers. Prepreg must have the same dielectric constant as core in order to maintain proper impedance control between all layers. Core and prepreg alternate in multilayer boards.

The multilayer process starts with core material and copper on both sides. The inner layer surfaces are first etched, while the outer surface layers remain fully copper-plated. The cores are then stacked together with prepreg. After heating and curing, the dielectric constant of both materials becomes the same value. Since prepreg partially melts during this process, traces adjacent to the prepreg will sink into the glue material. Trace separation between two layers is reduced by twice the thickness of a single trace. This separation occurs because the glue spreads out over the traces. Solid planes do not sink into the prepreg. After final assembly, any prepreg that has been squeezed out of the sides of the PCB will be trimmed away.

After curing, via holes are drilled. This drilling exposes the copper layers and pads throughout the assembly, although connection is not made until a plating material is inserted into the holes. This plating material covers both the inside and outside surfaces of the board simultaneously. During this plating process, a mask is applied to protect the PCB's outer layer except for traces and via holes. After plating, outer traces will have accumulated approximately 0.5-oz of copper. Impedance calculations for outer layer traces must be calculated for a trace thickness of 1.5 oz, if a 1 oz copper laminate is provided. After plating, the rest of the top layer is etched away, leaving a finished product. The PCB is then protected with soldermask or conformal coating and silk-screened.

Figure 8.17 shows a sample ten-layer stackup to illustrate how a PCB designer can specify details related to the manufacturing process of the PCB.

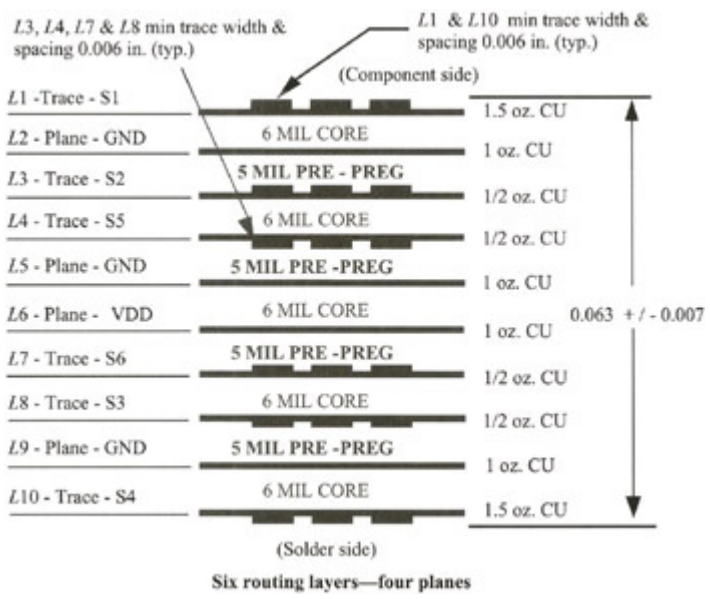
L3, L4, L7 & L8 min trace width & spacing 0.006 in. (typ.)
L1 & L10 min trace width & spacing 0.006 in. (typ.)
(Component side)
L1 -Trace - S1
1.5 oz. CU
L2 - Plane - GND
6 MIL CORE
1 oz. CU
L3 - Trace - S2
5 MIL PRE - PREG
1/2 oz. CU
L4 - Trace - S5
6 MIL CORE
1/2 oz. CU
L5 - Plane - GND
5 MIL PRE -PREG
1 oz. CU
L6 - Plane - VDD
6 MIL CORE
1 oz. CU
0.063 +/- 0.007
L7 - Trace - S6
5 MIL PRE -PREG
1/2 oz. CU
L8 - Trace - S3
6 MIL CORE
1/2 oz. CU
L9 - Plane - GND
5 MIL PRE -PREG
1 oz. CU
L10 - Trace - S4
6 MIL CORE
1.5 oz. CU
(Solder side)
Six routing layers—four planes

Figure 8.17: Sample ten-layer PCB stackup definition.

In Fig. 8.17, all signal layers are ½ oz. copper, while the reference planes (voltage and ground), are 1 oz. The outer layer starts with 1 oz copper. After plating, however, final thickness becomes 1.5 oz. For functionality purposes, 1 oz copper is usually required, or two times the thickness of the signal planes. This is because power planes must provide large amounts of voltage and return currents to all components simultaneously. To prevent overheating due to a large voltage (*IR*) drop within the plane, caused by power consumption of all components, an additional layer of ½ oz of copper is required.

In a multilayer board, start by defining the core. These inner layers are generally the reference planes (power and ground potential). If designated as signal planes, etching is performed to define the trace structure. The thickness between the opposing layers and core depends on the thickness of the original laminate. If the overall height dimension of the board is 0.062 in. (1.6 mm), the thickness of the core for a four-layer stackup will be greater than the spacing for a higher density board. This is because with more layers, a smaller physical distance between layers must occur to

maintain the same overall height dimension. With a smaller distance between layers, the trace width must be altered to maintain desired impedance (see in Chapter 4). An example of height distance variation for various stackup schemes is shown in Fig. 8.18.

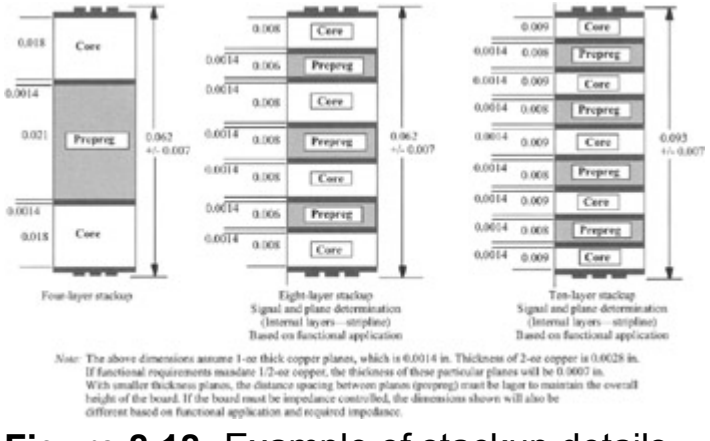

Figure 8.18: Example of stackup details.

For high-speed applications, the power and ground plane(s) must be located as close together as possible. This creates an internal decoupling capacitor that removes switching currents injected into the power distribution network, preventing RF energy from being created and propagated throughout the structure.

If additional planes are required, these planes should be at ground potential. It is common practice to have one power plane and multiple (two, three or more) ground planes. Multiple planes at the same potential allow return currents within the reference plane to mirror image themselves throughout a trace route, provided the signal trace is routed adjacent to the same reference plane. If return current jumps between planes, these currents will not have a low-impedance path back to the source, thus exacerbating the development of RF energy. The multiple ground planes must be connected together in as many places as possible, with ground vias, if component ground pins are not located in close proximity to each other throughout the entire board.

Soldermask must not be used on any *ground stitch* or mechanical securement connection to chassis ground. This includes ground points (chassis ground screws, gaskets), I/O bulkhead connectors, I/O adapter bracket mounting holes, ESD guard band, and localized planes on both the component (top) and solder (bottom) layers. Soldermask prevents RF bonding between critical ground connections and mounting securement hardware.

All unconnected vias must be removed from the artwork prior to production of the film. An unconnected via is defined as a pad on a plated through-hole that has no physical connection to any trace on any signal layer. This requirement does not apply to intentionally implemented ground vias that are provided for layer jumping RF return current. The PCB designer must perform this removal process prior to sending out film or gerber files for processing. When a guard trace has been pulled away from a signal trace by a via, pin escape, or through-hole device, there must be no connection to this via on that layer. (Connection to this via must be made on a different layer.)

For compliance with product safety standards, use of flame retardant material for the fiberglass assembly material is mandatory. This requirement prevents the possibility of fire occurring should a high-temperature level be applied to the board material. Fire results due to a combination of high temperature, combustible fuel, and oxygen. If a power resistor or component generates high levels of thermal energy, the core material could burst into flames, thus causing potential harm to the user or environment, if a fire enclosure barrier is not provided to retain the flames until the source of fuel get used up. A flammability rating of V-1 or V-0 is the minimal required, mandated by international safety agencies. The vendor's logo, date code, and flammability rating must also appear on the bare board on either the top or bottom layer in order to satisfy traceability of the material as being appropriate for the intended application. This identification requirement applies to the board fabricator only. However, a notation on the fabrication drawing must indicate this requirement.

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Appendix A - Summary of Design Techniques

Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, Second Edition

by Mark I. Montrose

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Appendix A: Summary of Design Techniques

CHAPTER 1: —INTRODUCTION

1. Application and use of the product should be considered for a specific environment—residential, commercial, light industrial, heavy industrial, medical, telecommunications, and so forth. This environment includes three areas of concern related to the EMC environment: source, propagation path, and receptor (1.2).

2. Five considerations exist when defining an EMC event: frequency, amplitude, time, impedance, and dimensions (1.3).

3. Test requirements and standards change on a frequent basis. It is difficult to keep up to date with a constantly changing regulatory environment. Before implementing tests, and the need to comply, the latest publication issue and mandatory date of compliance must be verified (1.4–1.7).

4. European requirements differ from those of North America and other countries throughout the world (1.5–1.7).

5. Emissions refer to energy that leaves a product. Immunity ensures that a product is not disrupted by externally induced events. Different tests are required for immunity and are mandatory only for certain countries around the world. The need for and current requirements prior to implementing expensive or additional components or design to minimize potential immunity events must be verified (1.6–1.7).

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CHAPTER 2: —PRINTED CIRCUIT BOARD BASICS

1. Passive components contain hidden behavioral characteristics. Design engineers generally select a component for use only in the time domain or at DC voltage levels. Because of digital logic transition between high- and low-voltage levels, an AC switching element will coexist based on the mathematics of the Fourier transform. This AC element is identified as RF energy. Due to parasitics (characteristic behavioral features within a device, such as capacitance between windings of an inductor or capacitance between the leads of a resistor), various effects will be observed. These effects are frequency dependent and become more serious as frequency increases (2.1).

2. One should never assume that a resistor is a resistor, a capacitor is a capacitor, or an inductor is an inductor when used with digital components (2.1).

3. The field of EMC is based on Maxwell's equations. An understanding of how Maxwell works is all that is required, *not* solving equations that are complex and requires knowledge of calculus. Maxwell's equations can be simplified using Ohm's law, which is not mathematically perfect. However, it helps explain in simple terms the fundamental concept of EMC (2.2).

4. For a circuit to operate, a closed-loop network must be present. For the time domain, the return current (after reaching the load) will find its way home through the power distribution network. This same signal in the frequency domain must also find its way back home to satisfy Maxwell, Kirchhoff's, and Ampere's equations and laws, except that it may do so through free space instead of metallic interconnects (wire, traces, etc.) (2.2).

5. In order to minimize the development and propagation of magnetic flux, or RF energy, it is mandatory that a signal trace be positioned as close as possible to its return path. If magnetic flux travels counterclockwise in one direction and clockwise in another, a cancellation effect will be observed. The greater the cancellation, the less RF energy will be present to cause harmful disruption (2.3).

6. A stackup topology must be used that is appropriate for a given design: microstrip or stripline. Microstrip topology refers to traces located on the outer layers of a stackup assignment. Stripline refers to layers internal to the PCB, with reference planes on both sides. Each topology has advantages and disadvantages, depending on the application and number of nets to route (2.4).

7. Where three or more reference planes are provided (e.g., one power and two ground planes), optimal performance of high-speed signal traces *may be achieved* when routed adjacent to a reference plane at 0V-reference, *not* adjacent to the power plane. The reason for this statement is one of the basic fundamental concepts of designing EMI suppression within a PCB (2.5).

8. A ground plane incorporated as the first layer within a multilayer stackup (Layer 2), instead of the power plane, will provide for enhanced suppression of RF energy owing to reduced parasitic capacitive coupling to the enclosure (2.5).

9. The use of single-sided PCBs is generally reserved to products that

do not contain periodic signals (clock) or are designed for use in analog instrumentation and control systems. Because of the limited ability to place components in an optimal manner for short trace lengths, as well as the need for both a power and ground system, a best case attempt to layout the board must occur (2.5.1).

10. The following requirements are mandatory for *single-sided* design (2.5.1):
    - Identify all power and ground sources, along with critical signal nets.
    - Partition the layout into functional subsections. Take into consideration the requirements of sensitive components and their physical relationship to I/O ports and interconnects.
    - Position all components with critical signal nets adjacent to each other.
    - If different ground nodes are required, determine if they are to be connected together, and if so, where.
    - Route the rest of the board, keeping in mind the need for flux cancellation for traces rich in RF spectral energy, along with the need for ensuring that a RF return path is available at all times.
    - Route all power and ground traces adjacent (parallel) to each other in a *radial fashion* from the power supply to all components. Minimize total physical routed length of the trace route. This minimizes loop currents that may be developed by high-frequency switching noise (internal to the components) from corrupting other circuits and control signals. Ideally, the only time these traces should be separated by a distance greater than the width of any individual trace is when they must separate for connection to the decoupling capacitor. Signal flow should parallel these return paths.
    - Prevent loop currents by not tying different branches of a tree to another branch.

11. Design and layout considerations for *double-sided* assemblies are as follows (2.5.2):
    - Place a return or guard trace as physically close to the high-threat signal trace as possible to permit RF energy to complete its return to the source. The power and ground return must be routed parallel to each other, with decoupling capacitors provided for each and every component that injects switching energy into the power distribution system. With this topology, difficulties in routing may occur. However, significant benefits will be observed related to EMC compliance.
    - Use a gridded power and ground layout to minimize inductance in the RF return path. The smaller the grid, the better the performance.
    - Remember that there is no such thing as a truly EMI compliant double-sided PCB. The physical distance spacing between the ground plane on the bottom of the board and a signal trace on the top layer is extremely large. Treat all double-sided designs as two single-sided assemblies, with techniques for ensuring that a RF return path is physically adjacent to all high-threat signal traces.

12. Regarding multilayer stackup assignments, the recommendations provided in this section must be followed. Understand the concept presented for ensuring that a solid plane is adjacent to each routing layer (2.5).

13. Radial migration deals with the transfer of electromagnetic energy from a high-bandwidth section, such as a CPU or frequency-generating circuits, to lower speed sections, which include I/O interconnects. This slowing of signal propagation occurs because all components have input capacitance and internal propagation delay. In addition, use of slower speed components is generally provided for I/O interconnects (2.6).

14. For many circuits, differential-mode energy is required for transferring electrical intelligence between components. All components use a common reference point. Any imbalance in the transfer of energy in the transmission line will cause common-mode energy to be developed within the network. Common-mode currents are the primary source of undesired RF energy. A very small amount of common mode energy developed is a significantly greater than

differential mode by many orders of magnitude (2.7).

15. One design and layout technique to reduce common-mode current is to reduce the physical distance spacing between signal trace and RF return path, not just the DC return path (2.7).

16. RF current on a source trace will create a mirror image in a return plane. This projection will spread out within the return path. This spread means that the current density distribution will be greatest directly under the trace, with less energy present in the plane at a distance farther away. Knowledge of this current spread is important to prevent common-impedance coupling (crosstalk) in the RF return path (2.8).

17. An optimal grounding assignment, product dependent, must be selected based on series, parallel, single point, multipoint, or a combination of different technologies (2.9.):
    - Use single-point grounding for low-frequency applications (audio, analog instrumentation, 50/60 Hz power systems, etc.) with clocks 100 kHz and slower (2.9.1).
    - Use multipoint grounding for systems operating above 100 kHz. Multipoint grounding minimizes ground impedance present within the power distribution system by shunting RF currents from planes containing RF energy to chassis ground (2.9.2).

18. Use of multipoint grounds may allow resonances to be developed between ground points. These resonances exist by virtue of parasitic capacitance between the PCB and chassis, and inductance between ground points along with the inductance within the screw securement means of the assembly (2.9.2).

19. Ground loops contribute significantly to the development and propagation of RF energy. This return path develops a voltage potential difference between two locations, increasing RF losses in the return path (2.10).

20. RF ground loops will develop a voltage potential difference between two components, regardless of whether inductance exists between these points. Inductance in a transmission line causes magnetic coupling of RF current to occur between a source and victim circuit, increasing RF losses in the return path (2.10).

21. RF ground loops must be minimized between (2.10)
    - High RF energy circuits and system ground.
    - Functional subsections.
    - Multipoint ground locations.
    - I/O interconnects and associated control circuitry.
    - Power supply input terminals and system ground.
    - Card edge connectors and main system ground.
    - Opposite edges of the PCB.
    - Cable shields and chassis ground.

22. The distant spacing between all ground locations is calculated based on a straight-line distance not exceeding $\lambda/20$ of the highest frequency generated on the board. A ground stitch is placed in the middle between these two ground point locations (2.11).

23. Creative techniques may be available for implementing multipoint grounding, taking into consideration aspect ratio and distance spacing between ground locations (2.11).

24. A signal routing plane must always be located adjacent to a solid *image* or *return* plane. This plane allows RF return currents to have a low-impedance path back to its source, while mirror imaging its source trace. The closer the distance spacing, the more flux cancellation will occur (2.12).

25. One should never place three or more routing layers adjacent to each other. Each routing layer must be adjacent to a solid reference plane (2.12).

26. Vias placed in an image plane do not degrade the imaging capabilities, except where continuous slots are provided. Vias do, however, affect other functional parameters in a PCB layout. These

functional parameters include the following (2.12):

- Reducing interplanar capacitance; degrades decoupling efficiency.
- Prevents RF return currents from jumping between routing or image planes.
- Adds more inductance and capacitance into a trace route.
- May create an impedance discontinuity within the transmission line structure.

27. There must be optimal coupling of magnetic flux between both source and return when connectors are used (2.12).

28. A solid image plane must never be violated with a trace route. Moats are acceptable in an image plane, provided the adjacent routing layer does not have traces crossing the moat (2.13).

29. Oversized through-holes or vias prevent RF return current from traveling back to its source in an optimal, low-impedance manner (2.13).

30. Inductive trace length from component leads is minimized by not using sockets for through-hole devices (2.13).

31. A bypass capacitor may be used to jump across a moat to allow RF return current to travel back to its source. This capacitor must be located immediately adjacent to the source trace (2.13).

32. The PCB can be partitioned into functional areas; high bandwidth areas are separated from medium and low bandwidth; each section can be isolated using partitions or moats, if required (2.14).

33. Each partition must be grounded to chassis in as many locations as possible to minimize ground and signal loops (2.14).

34. Calculating the physical wavelength of RF energy is extremely easy (2.15).

35. An appropriate logic family must be chosen for functionality purposes. High-speed components are not to be used when another logic family with a slower edge rate is acceptable. Various concerns exist when specifying and using digital components related to both time and frequency domain concerns (2.16).
    - Manufacturers of components rarely specify in data sheets the minimum edge rate transition of digital devices. Usually, only the average or maximum rise- and fall-time transitions are provided. Minimum edge rate transitions are the primary source of EMI. If in doubt, measure actual edge rate with a high-bandwidth oscilloscope. Make the component selection based on measured results, and not on published data, which is generally incorrect.
    - Determine the maximum amount of peak inrush surge current for digital components when transiting logic states under maximum capacitive load. A digital device sends (sources) current to multiple loads. Each load is capacitive. Current must travel through the device (from the power pin) to all output pins during a transition state. The existance of many loads on a net means that a large amount of current is required from the power distribution network traveling through the device. Under a maximum load condition, a significant bounce of the power and ground structure will occur, causing common-mode energy to be developed and propagated throughout the PCB assembly.
    - Components with fast edge rates generate a greater amount of spectral bandwidth RF energy than devices with a slightly slower edge rate.
    - Harmonics of the primary switching frequency must be considered when determining the spectral profile of digital components.

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CHAPTER 3: —BYPASSING AND DECOUPLING

1. The capacitor must be selected based on intended use and application: decoupling, bypass, or bulk.

2. Bypassing and decoupling are functions of circuit resonance. Determine if the circuit is a series, parallel, or parallel *C*-series *RL* network. Calculate resonant frequency when using a capacitor for this particular function (3.1).

3. Decoupling capacitors must be provided on circuits that contain high-frequency RF switching energy. Calculate capacitance value for optimal performance and frequency range of interest. Interests include the value of capacitance, impedance, equivalent series inductance, equivalent series resistance, and energy storage. Do not guess values or use the same value from previous designs, such as 0.1 μF (3.1–3.2).

4. The inductance value of the lead lengths of radial and axial capacitors must be included when determining use for a particular resonant frequency. Include the total amount of equivalent series inductance and equivalent series resistance internal to the capacitor (3.2.1).

5. An understanding of various types of capacitor families, and their applications, is essential (3.2.2).

6. When selecting a decoupling capacitor, one must take into consideration the point source charge that a logic device requires to ensure functionality when multiple components switching logic state for all pins simultaneously under maximum capacitive load (3.2.3).

7. Capacitors decouple RF energy up to their point of self-resonance. Above self-resonance, the capacitor appears inductive to the circuit. When the capacitor goes inductive, its effectiveness as a decoupling element decreases (3.2.4).

8. In a capacitor, the dielectric material is one factor in determining the magnitude of impedance at the self-resonant frequency desired. All dielectric material is temperature sensitive. The capacitance value will change in relation to ambient temperature (3.2.4).

9. Surface mount capacitors have a higher self-resonant frequency than through-hole. This is because there is a significantly less amount of inductance within the device package (3.2.4).

10. When the power or ground trace and lead inductance are combined, a higher impedance value will be presented between the component's pin and its respective reference plane, which is undesirable. With traces being inductive, a voltage gradient is developed between two sources, creating undesirable RF development of common-mode energy (3.2.4).

11. Parallel capacitors can be used to decouple a larger bandwidth of RF spectral energy (3.3).

12. When selecting parallel capacitors, it is important to remember that as the larger value capacitor goes inductive, the smaller value capacitor is still capacitive. At a particular frequency, a *LC* circuit is developed between the two capacitors. An infinite impedance could be

generated with no decoupling benefit provided. When this occurs, single-capacitor decoupling is all that one can use for this application (3.3).

13. Printed circuit boards generally have a self-resonant frequency well above 50 MHz. This built-in decoupling capacitor (power planes) should be used to maximum advantage (3.4).
    - Calculating the value of planar capacitance is easy (3.4.1).
    - Power planes generally provide an adequate low self-resonant frequency decoupling for standard TTL components (3.4.1).

14. If the self-resonant frequency of the power and ground planes is the same as the self-resonant frequency of the lumped total of all discrete decoupling capacitors installed, there will be a sharp resonance where these two frequencies meet. No longer will there be a wide spectral distribution of decoupling (3.4.1).

15. One simple method to change the self-resonant frequency of the power and ground planes is to change the distance spacing between planes or their physical size (area). Increasing or decreasing the height separation, relocating within the layer stackup, or making the planes a different physical size will change capacitance value (3.4.1).

16. For frequencies above self-resonance, additional decoupling provides no additional benefit as long as the switching frequencies of the components are within the decoupling range of the power and ground plane structure (3.4.2).

17. Although good distributive capacitance exists when using a power and ground plane structure, adjacent close stacking of these planes plays a critical part in the overall PCB assembly (3.4.3).

18. Buried capacitance is a patented manufacturing process in which the power and ground planes are separated by a 0.001 in. (0.025 mm) dielectric. With this small dielectric spacing, decoupling is effective up to 200–300 MHz. Above this frequency range, use of discrete capacitors may not perform as well as buried capacitance in decoupling digital components (3.4.4).

19. Multilayer PCBs contain one or more pairs of voltage and ground planes. These planes function as a low-inductance capacitor, preventing the creation of RF currents generated from components switching logic states. Multiple chassis ground connections to all ground planes minimize voltage gradients between board, chassis, and between/among board layers. These gradients also are a major source of common-mode RF fields (3.5.1).

20. Before determining where to locate decoupling capacitors, the physical structure of a PCB must be understood. The impedance of the PCB power and ground distribution network must be minimized. The easiest way to minimize resistive and inductive components of the network is to provide solid planes (3.5.2).

21. If the impedance of the loop is smaller than the rest of the system, some fraction of high-frequency RF energy will transfer or couple to the larger loop formed by the power distribution system. With this situation, RF currents are developed in the loop structure and, hence, higher EMI emissions (3.5.2).

22. Decoupling capacitors must be provided for devices with edges faster than 2 ns and should be provided, placement wise, for every component (3.5.3).

23. Placement of 1 nF (1000 pF) capacitors (capacitors with a very high self-resonant frequency) on a 1 in. (2.54 cm) grid provides additional decoupling of RF currents for both signal traces and the power planes, especially if a high-density PCB stackup is provided (3.5.3).

24. Various techniques are available for placement of decoupling capacitors. The optimal configuration is the one with the least amount of lead inductance (3.5.3).

25. Where very high-frequency performance is required, multiple vias to the power and ground plane, along with short, fat traces reduce the

overall inductance of the circuit. Using an increased size of SMT pad with multiple vias to the plane makes a significant improvement in high-frequency performance (3.5.5).

26. A technology known as microvias permits use of vias embedded within component mounting pads. These vias have very low inductance. A negative aspect of using microvias is that power cannot be efficiently transferred through microvias, hence mandatory use of a trace from the component pad to the power and ground network (3.5.6).

27. It is common to select a decoupling capacitor for a particular application, usually the first harmonic of a clock or processor. Sometimes a capacitor is selected for the third or fifth harmonic, since this is where a majority of RF current is observed (3.6.1).

28. When performing component placement on a PCB, one should make physical provisions for adequate high-frequency RF decoupling. One should also verify that all bypass and decoupling capacitors chosen are selected based on intended application. This is especially true for clock-generating circuits (3.6.1).

29. Capacitors can be used to shape the waveform of signal traces. The capacitor, *C*, alters the signal edge (slew rate) by rounding the time period the signal edge transition takes to change from logic state "0" to logic state "1" (3.6.2).

30. Bulk capacitors ensure that a sufficient amount of DC voltage and current is available to components, especially when digital devices switch data, address, and control signals simultaneously under maximum capacitive load (3.6.3).

31. A sufficient quantity of bulk capacitors must be used to provide a localized source charge of DC voltage and current. This is required for components that consume large amounts of power when all pins switch simultaneously under maximum capacitive load. Generally, a decoupling capacitor will perform the function of both bulk and RF current suppression (3.6.3).

32. Bulk capacitors must be used at all power connectors and at opposite or far ends of the board. Also, bulk capacitors must be located at the furthest location from the power entry connector. This is in addition to all components that consume large amounts of DC voltage and current. Bulk capacitors minimize DC voltage and current fluctuations (dropout or droop) which cause degradation of circuit functions (3.6.3).

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CHAPTER 4: —CLOCK CIRCUITS, TRACE ROUTING, AND TERMINATIONS

1. A transmission line is another word for PCB trace. A PCB is defined as a rigid structure for supporting transmission lines sharing a common substrate (4.1).

2. Two basic topologies are available for developing transmission line structures within a PCB. Each topology has several configurations: microstrip (single and embedded) and stripline (single, dual, symmetrical, or asymmetrical). Another topology, co-planar, can be implemented as both microstrip and stripline (4.1).

3. High-speed traces must be impedance controlled. Calculations to determine optimal trace width and distance to the nearest reference plane must occur prior to board layout. Board manufacturers and CAD programs can easily perform these calculations (4.1).

4. Formulas commonly used to calculate transmission line impedance are approximate and generally never reflect actual values. This approximation value is due to tolerances that arise during the production cycle and to first- and second-order effects (trace thickness, side wall shape, solder mask coverage, mixed dielectrics, and the like), all of which can vary widely. Sensitivity analysis should be considered if high accuracy is required (4.2.1–4.2.5).

5. The velocity of propagation of an electromagnetic field within a transmission line is based exclusively on the dielectric constant of the board material (4.2.1–4.2.5).

6. Differential traces are two conductors physically adjacent to each other throughout the entire trace route. The impedance for differential (paired) traces is *not* the same as a single-ended (differential-mode) trace. For this configuration, the line-to-reference plane characteristic impedance is for *single-ended* routing, *not differential-pair*. In order to calculate differential-pair impedance, the single-ended impedance value *must be known* ahead of time (4.2.5).

7. Vias or other discontinuities, such as connector pins, cannot be placed between routed trace pairs (4.2.5).

8. Two types of differential pair configurations exist: edge-coupled stripline and broadside-coupled stripline. Each configuration has unique characteristics (4.2.5).

9. Significant advantages exist related to differential pair routing. Differential pairs must be routed as close together as is physically possible (minimal line-line spacing) using matched trace length. Trace lengths do not need to be exact, since the speed of propagation of the signal trace is the important element for the trace length of differential pairs. A few picosecond skew between traces will not affect performance for many designs operating below 1 GHz (4.2.5).

10. Section (4.2.5) contains a detailed list of the advantages of routing differential pair traces.

11. A transmission line (PCB trace) allows signals to propagate at or near the speed of light within a medium, modified (slowed down) by

capacitance and the dielectric constant (ϵ_r) of the transmission line (4.3).

12. The relative permittivity (dielectric loss) is a measure of the electrical properties of the medium that an electromagnetic wave propagates or travels through. The larger the dielectric value, the slower the signal (propagation) between two points (4.3).

13. Velocity of propagation and dielectric constant are reciprocals of each other, and are used to describe signal propagation (4.3).

14. When using a value for dielectric constant (ϵ_r) to calculate trace impedance, or for use with other equations, the proper numeric value must be used. PCB materials have different values for dielectric constant. Some material has a consistent value of ϵ_r throughout the frequency spectrum, while other material, such as FR-4, varies with frequency (4.3).

15. When performing calculations for impedance, a different value of ϵ_r may be required for each trace route, depending on the speed of operation and frequency of use (4.3).

16. A trace that has many capacitive loads will slow down the velocity of signal propagation. This delay in propagation may cause signal integrity concerns (skew) to occur (4.4).

17. Components add capacitance to the trace route. The larger the value of capacitance, the lower the impedance of the transmission line. A lower impedance means that additional drive current is required (Ohm's law), exacerbating EMI (4.4).

18. When placing components on a PCB during layout, the following concerns exist (4.5):
    - Locate clock circuits near the center and/or a ground stitch location (to chassis ground) on the PCB rather than along the perimeter or near the I/O section. If the transmission line goes to a daughter card, ribbon cable, or peripheral located remote from the main PCB, terminate the transmission line directly at the connector or boundary location. It is imperative that this trace route be a point-to-point radial.
    - Never use sockets for components that have periodic signal transitions. Sockets add lead inductance. This additional inductance establishes a voltage potential difference between two points, which in turn causes common-mode energy to be developed.
    - If a socket must be used, include total value of lead inductance to any equation when using simulation tools. The length of the lead must also be included in the analysis for trace length calculations.
    - For a clock area, route only traces associated with this circuitry within this localized section.
    - Allow for possible use of a Faraday shield (a metal enclosure that covers devices 100%) around the entire clock circuit area. Provide for a ground trace circumscribing the zone (except for the point of signal trace exit, if required). This shield must be of a RF type similar to those used in UHF and microwave applications.
    - When placing PCB components during layout that use clocks or periodic signals, locate these devices so that periodic signal or clock traces are routed for a best straight-line path possible with minimal length and number of vias. Vias add inductance to the trace, approximately 1–3 nH each. Inductance in a trace may cause signal integrity concerns and potential RF emissions.
    - If a periodic signal or clock trace must traverse from one routing plane to another, make sure this transition occurs at a component lead (pin escape) and not anywhere else, if possible.
    - Do not locate clock signals near I/O areas. For traces within 2 in. of I/O, use the slowest speed logic device available. For traces within 3 in. of I/O circuits, use medium speed logic. This requirement is not needed when functional partitioning is implemented.

19. Reflections are unwanted byproducts in digital logic designs.

Reflections within a transmission line contain both overshoot and ringing before stabilizing to a quiescent level and are a manifestation of the same effect. Overshoot is the effect of an excessive voltage level above the power rail or below the ground reference. Undershoot is a condition where the voltage level does not reach the desired amplitude for both maximum and minimum transition levels (4.6).

20. Reflections are created when significant impedance mismatches exist in a transmission line between source and load (4.6).

21. Reflections from signals on a trace are one source of RF noise within a network. Reflections are observed when impedance discontinuities exist in the transmission line. These discontinuities consist of (4.6)
    - Changes in trace width.
    - Improperly matched termination networks.
    - Lack of terminations.
    - T-stubs or bifurcated traces.
    - Vias between routing layers.
    - Varying loads and logic families.
    - Large power plane discontinuities.
    - Connector transitions.
    - Changes in impedance of the trace.

22. The PCB layout designer must determine if a physical trace route is electrically long. If the trace is electrically long, termination may be required (4.7).

23. If traces must be electrically long, the trace must be routed using transmission line techniques (4.7).

24. Simple formulas exist to determine if a transmission line is electrically long during component placement and preliminary routing (4.7).

25. When routing traces, the following must be considered (4.8):

    For single-ended transmission lines:
    - Do not daisy-chain traces for ease of routing, unless the distance is small between loads, with respect to propagation length and signal edge transitions.
    - Route using radial connections, which is a single point-to-point connection from a driver capable of sourcing multiple loads simultaneously. Do not daisy-chain. Each component must have its respective trace terminated in its characteristic impedance.
    - If a trace is electrically long, provide for termination appropriate for the routing topology.
    - If at all possible, do not use T-stubs, as signal integrity problems will develop.

    For differential pair signaling, four concerns exist when routing between layers (4.8.2):
    - *Impedance control*. When jumping layers, an impedance discontinuity is injected into the transmission line. This impedance discontinuity may cause reflections to occur if termination is not properly chosen.
    - *Return currents and layer jumping*. Flux cancellation for return currents may not be optimal, especially for certain configurations.
    - *Velocity of propagation*. Traces routed microstrip will have their electromagnetic fields propagate faster than stripline.
    - *Development of common-mode energy*. If a receiver is not the immediate load, but through interconnects to a cable or connector assembly (e.g., backplane configuration), an additional capacitive load will be presented to the trace. This capacitive load can cause differential-mode signals to be converted to common-mode signals at the boundary location, exacerbating EMI.

26. When routing traces, the following are to be noted (4.9):
    - Route clock traces on one routing plane only. This layer must be adjacent to a solid (image) plane at all times. If possible, route all clock traces stripline. Traces on the outside of the board are microstrip (4.9.1).
    - Be aware that the impedance of a transmission line (trace) will be different for microstrip and stripline, assuming the same line width is used.

- Use a solid image or reference plane/trace adjacent to the signal route. Minimize trace length routing while maintaining a controlled impedance value of the transmission line.
- If a series termination resistor is used, connect the resistor directly to the pin of the driver without use of a via between resistor and component. After the resistor, *now* place a via to the internal stripline layers.
- Do not route clock or other sensitive traces microstrip layer on a multilayer board.
- If we maintain constant trace impedance and minimize or eliminate use of vias, the trace will not radiate any more than a coax.

27. Three phenomena by which planes and, hence, PCBs create EMI are as follows (4.9):
    - Discontinuities in the image plane due to use of vias and jumping clock traces between layers.
    - Peak surge currents injected into the power and ground network (image planes) due to components switching signal pins at the same time to propagate throughout the PCB.
    - Flux loss into the annular keep-out region of vias if *3-W* routing is not provided for the trace route. Distance separation of a trace from a via must also conform to *3-W* spacing.

28. Microstrip allows for faster transition of signal edges, while also permitting a greater amount of RF current to radiate from the traces (4.9.1).

29. Stripline allows for optimal suppression of RF current, but at the expense of slowing down signal edges (in the picosecond range) due to capacitive loading between the trace and surrounding planes (4.9.1).

30. If traces must jump between planes, ground vias must be used at each and every layer jump to maintain image plane continuity (4.9.2).

31. The ground pin of a component can also be used as a ground via (4.9.2).

32. Crosstalk refers to unintended electromagnetic coupling between traces, wires, trace-to-wire, cable assemblies, components, and other electrical devices susceptible to electromagnetic field disturbance (4.10.1).

33. The main concern with crosstalk, related to parallel traces, is to prevent electrical noise on one trace (source trace) from causing harmful interference to a victim trace (4.10.1).

34. To prevent crosstalk, the design and layout techniques listed below are useful during PCB layout (4.10.2):
    - Group logic families according to functionality. Keep the bus structure tightly controlled.
    - Minimize the physical distance between components during placement.
    - Minimize parallel routed trace lengths.
    - Locate components away from I/O interconnects and other areas susceptible to data corruption and coupling.
    - Provide termination for impedance-controlled traces, or traces rich in RF harmonic energy.
    - Avoid routing of traces parallel to each other. Provide sufficient separation between traces to minimize inductive coupling effects.
    - Route adjacent layers (microstrip or stripline) orthogonally. This prevents capacitive coupling between adjacent layers.
    - Reduce signal-to-ground reference distance separation.
    - Reduce trace impedance and signal drive level.
    - Isolate routing layers that must be routed in the same axis by a solid planar structure (typical of backplane stackup assignments).
    - Partition or isolate high noise emitters (clocks, I/O, high-speed interconnects, etc.) onto different layers within the stackup assignment.
    - Provide a band-limiting filter on specific transmission lines to prevent RF frequencies from coupling between source and victim traces.

35. The *3-W rule* minimizes crosstalk within a PCB per the following (4.11):
    - To minimize coupling between transmission lines or PCB traces. The rule states that *the distance separation between traces must be three times the width of a single trace measured from centerline to centerline*. Otherwise stated, *the distance separation between two traces, edge to edge, must be greater than two times the width of a single trace*.
    - Use of the *3-W rule* is mandatory for only high-threat signals, such as clock, differential pairs, video, audio, reset line, or other system-critical nets. Not all traces within a PCB have to conform to *3-W* routing. It is important to determine which traces are to be classified as critical.
    - Use of the *3-W rule* should not be restricted to clock or periodic signal traces. Differential pairs (balanced, analog, ECL, and similar sensitive nets) are also prime candidates for *3-W*. The distance between paired traces must be *1-W* for the differential traces and *3-W* from each of the differential pair to adjacent traces (4.11).

36. Guard traces must be at 0V-potential surrounding clocks, periodic signals, differential pairs, or system-critical (high-threat) traces from source to destination. Shunt traces are traces located directly above or below a high-threat trace that parallels the trace along its entire route (4.12).

37. For guard and shunt traces (4.12)

    The primary function of guard and shunt traces is to provide an alternative return path for RF currents to return to their source, if a solid image plane is not provided as in multilayer assemblies. This includes the following reasons:
    - To enforce the *3-W rule*.
    - To prevent common-mode RF coupling from a high-threat signal trace to other circuit traces (minimize crosstalk).
    - To provide a low-impedance alternative RF return path and to minimize RF common-mode currents that may be developed within the transmission line.
    - To create an impedance-controlled, coaxial-based transmission line for specific nets.
    - Guard traces are commonly found on single- and double-layer boards (e.g., those without power or ground planes).
    - Shunt traces perform best in multilayer boards (six or more layers).
    - Place a guard trace around every clock line if the trace on the board is routed single- or double-sided (no ground plane present). Make the distance spacing as close as possible between the signal and guard trace.
    - When using guard and shunt traces, make connections to the ground planes at irregular intervals throughout the route. Symmetrical grounding may allow a tuned circuit to be developed that can resonate at a particular harmonic or wavelength of a particular signal.
    - Do not route two different signals between guard traces, as crosstalk could develop. If the traces are paired (differential), then these two traces may be routed within the same guard trace.

38. Trace termination plays an important role in ensuring optimal signal integrity as well as minimizing development of RF energy; absorbs unwanted energy (4.13).

39. The need to terminate is based on several design criteria. The most important criterion is the existence of an electrically long trace. When a trace is electrically long, or when the length exceeds one-sixth of the electrical length of the edge transition time, the trace requires termination. Even if a trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing (4.13).

40. The easiest way to terminate is to use resistive elements. Two basic configurations exist; source or end. Several methodologies are available for these configurations. Refer to the referenced section for details of implementation:
    - Series termination resistor (4.13.1).
    - End termination requirements (4.13.2).

- Parallel termination resistor (4.13.3).
- Thevenin termination (4.13.4).
- AC (RC) termination (4.13.5).
- Diode termination (4.13.6).
- Differential signals (4.13.7).

Appendix A - Summary of Design Techniques

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CHAPTER 5: —INTERCONNECTS AND I/O

1. Most RF emissions in I/O circuitry are generated from (5.0)
   - Coupling of common-mode RF energy to I/O interconnects.
   - Power plane switching noise coupling into I/O circuits and cables.
   - Clock signals coupling to I/O cables through both conductive and radiated modes.
   - Lack of data line filtering on signals traces (both common mode and differential mode).
   - Improper connection of various ground methodologies (chassis, signal, frame, digital, and analog).
   - Use of unacceptable I/O connectors (plastic versus metal or unshielded versus shielded).
   - Ground potential difference between two circuits.
2. All metal connectors must be bonded 360 degrees to chassis ground, without use of a pigtail (5.0).
3. Driver and control logic must be located as close to the I/O connector as possible in order to minimize routed trace length and RF coupling of both common- and differential-mode currents to other signal lines (5.0).
4. Filter components must be provided in the trace route between control logic and I/O connector if the circuitry permits filters to exist (5.0).
5. Interconnects and I/O circuitry must be physically partitioned away from high RF bandwidth areas, especially the CPU area (5.1.1).
6. Provisions must be made for quiet areas by separating digital logic from analog circuitry along with their respective power and ground planes (5.1.2).
7. To implement a quiet area, use of a moat or partition is required. This quiet area can be implemented by (5.1.2)
   - I/O signals entering and exiting via an isolation transformer.
   - Data line filter.
   - A high-impedance common-mode inductor.
   - A ferrite material-based component.
8. Provision should be made in the artwork for inclusion of a fence to prevent radiated RF noise coupling between functional sections. This fence may also enhance system performance by preventing radiated crosstalk from occurring between component packages. At every ground location, one can bypass internally generated RF currents using a capacitor between the power and ground planes (5.1.3).
9. Depending on the placement of components, relative to susceptible circuits or I/O connectors, potential coupling of internal RF energy must be anticipated *before* routing traces or finalizing placement (5.1.3).
10. Noisy and quiet areas must be isolated through use of a partition or moat. A moat is an absence of copper on all layers: power, ground and signal. Connection between isolated areas is accomplished using data line filters, isolation transformers, or a bridge (5.2).
11. Techniques for preventing digital currents from corrupting analog circuits include the following (5.2):

- Isolate *all* plane layers along this partition line with absence of copper between these two regions. This absence of copper area is identified as a moat.
- For power and ground planes, use a 0.010 in. (0.25 mm) minimum wide moat.
- Tie analog ground and digital ground at ONE and only ONE point. This section of the ground plane will be the "bridge" that goes across the moat.
- Locate the analog portion of analog components exactly in the middle across the bridge.
- Permit no signals whatsoever to cross the moat in any location under any condition.
- Have any signals that must pass between the analog and digital sections travel *only* through the bridge and do so on a layer adjacent to the bridge (maintain RF return current path).
- Provide filters for analog power and phase lock loop circuits. This filter provides a digital noise-free analog power source.

12. When providing isolation between areas, care should be taken that all trace routing occurs in the common connection area and does not cross the moat (5.2).

13. Data line filters, ferrite beads, or isolation transformers are used for connection between noisy and quiet areas (5.2.1).

14. Two areas of concern for selection of components used in I/O circuits for isolation purposes are (5.2.1):
    - Proper bandwidth filtering.
    - Peak surge voltage capabilities for electrostatic discharge protection.

15. If filtering is required in an isolated area, these filter components must be located exactly across the moat. Both power and ground traces must be routed adjacent to each other to prevent potential RF ground loops that can be developed if both traces were located on opposite sides of the partition (5.2.1).

16. All copper layers in the area between a data line filter and connector should be removed. Removing the copper prevents coupling between filtered and filtered signals (5.2.1).

17. If analog or digital *power* is not required in an isolated area, this unused power plane can be redefined as a second ground plane, referenced to the main ground plane by vias in the isolated area (5.2.2).

18. Two types of filter configurations exist: capacitive and inductive. Different applications require one, the other, or both. Every I/O trace requires filtering; the exceptions permitted include fiber optic and certain types of local area networks and telecommunication interfaces. Filter components will not be effective unless their placement is exactly adjacent to their entry point (5.3.1).

19. Placement of bypass capacitors for I/O circuits must be determined before or after the data line filter. If located between the filter and I/O connector, the capacitor selected must have a voltage rating that will not be damaged when subjected to a fast transient of ESD event (5.3.1).

20. Provisions must be made for including bypass capacitors in I/O circuits. These capacitors can be used, if required, for compliance or functionality concerns (5.3.1).

21. All I/O brackets should be grounded to chassis ground unless single-point or isolated grounding is required. Also, this I/O bracket can be connected to the ground planes of the PCB, if the design permits. Provisions should be made for multiple connections from the ground plane to the bracket. This minimizes the aspect ratio between ground points for optimal loop control. If no external I/O connections exist on the adapter board, the chassis-mounting bracket must be isolated from signal ground (5.3.3).

22. For local area networks, data signals must be filtered with common-mode chokes if the protocol permits. Provision must be made for

complete isolation from digital switching noise from the main PCB using a moat (5.4).

23. For video, a filter must be provided between the controller and I/O, with the filter as close to the connector as possible. Provide isolated analog ground from digital ground through a ferrite bead if the device permits this type of ground connection. All analog traces and components must be connected over the analog isolated planes (5.5).

24. Constant trace impedance must be maintained for all signals routed in the video section. These traces may be a different impedance value from other traces on the assembly. A design technique for implementation involves removal of a reference plane (used for trace impedance), allowing the trace to be impedance controlled from another reference plane located at a further distance away within the stackup (5.5).

25. Certain vendors of video controllers tie analog ground to digital ground internal to the package. This connection may also be performed internal to the silicon die. If the RAMDAC chosen has these two grounds connected together, then it is imperative that a solid ground plane be used for both analog ground and digital ground. A ferrite bead must not be used for this particular type of RAMDAC. Other vendors have RAMDACs designed with *pure isolation* between analog ground and digital ground internal to the package. For these parts, a ferrite bead is used (5.5).

26. Audio interfaces are partitioned into three areas: digital, analog, and audio. The digital to analog connection must be made through a bridge located directly under the audio controller or as close to it as possible. All traces between digital and analog must be routed through this bridge, including analog power. The analog section must be isolated from the audio section by a second moat and additional data line filters. *Audio* ground must not be connected to *chassis or analog* ground. In addition, the signal return on unshielded audio cables must not be connected to analog or chassis ground (5.6).

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CHAPTER 6: —ELECTROSTATIC DISCHARGE PROTECTION

1. Electrostatic discharge (ESD) is a natural phenomenon that affects materials of different potential. This difference in potential occurs as a result of accumulated electric charges. Electric charges produce an electromagnetic field, which in turn can cause disruption to electrical equipment (6.1–6.2).

2. ESD is typically broken down into two primary types of discharge: human (direct) and furniture (air) (6.3).

3. Most ESD problems fall within two categories: component damage and operational disruption (6.3).

4. Four basic failure modes from an ESD event are related to PCBs (6.3):
   - Upset or damage caused by ESD current flowing directly through a vulnerable circuit.
   - Upset or damage caused by ESD current flowing in the ground circuit.
   - Upset caused by electromagnetic field coupling (indirect discharge).
   - Upset caused by a pre-discharged (static) electric field.

5. Design techniques for preventing damage to a PCB from an ESD event involve reducing field coupling. These include (6.4):
   - Use filters to attenuate the energy at the source.
   - Use filters to attenuate the energy received at the load.
   - Reduce coupling by separating components from each other.
   - Reduce coupling efficiency between source and load.
   - Reduce coupling efficiency by orienting susceptible devices perpendicular to areas susceptible to ESD corruption.
   - Install a metal shield over components and assemblies properly grounded.
   - Reduce electric field coupling by decreasing the impedance of the transmit and receive antenna.
   - Reduce magnetic field coupling by increasing the impedance of the antenna.
   - Couple signal lines to a ground structure.

6. The majority of direct ESD problems are cable related. The solution is straightforward—protect all lines, including signal, power, and the ground path (6.4).

   For single- and double-sided PCBs (6.4.1):
   - Power and ground traces must be routed adjacent to each other with minimal distance spacing between the two.
   - If multiple power and ground traces are required, they must be connected together in a grid fashion in as many locations as possible.
   - Parallel signal traces must be routed close together to minimize the RF return current loop area.
   - The signal trace must be routed as close to a ground trace as possible. A ground grid can help implement this requirement.
   - High-frequency bypass capacitors must be used between power and ground containing a low-impedance value at ESD frequencies. ESD is generally considered approximately a 300-

MHz event.

7. For multilayer assemblies, design techniques for ESD protection include the following, divided into three separated areas (6.4.2).

   For components:
   - *Spark gaps*. Spark gaps are sharply pointed triangles created within the copper of microstrip layers, aimed at each other. One trace is connected to one triangle, and ground is connected to the other. This is a poor technique for ESD control and should not be used with high-technology devices.
   - *High-voltage capacitors*. High-voltage disc-ceramic capacitors shunt ESD energy present on a signal line to ground.
   - *Avalance Diodes* (*Tranzorbs*™[1]). Avalance diodes (tranzorbs) are semiconductor devices specifically designed for transient voltage suppression applications.
   - *LC filters*. A *LC* filter is a combination of both an inductor and a capacitor connected in a desired configuration to chassis ground.
   - Non-ESD sensitive components must be selected, such as diode-protected CMOS or TTL for use in circuits susceptible to disruption.
   - Incorporate bypass capacitors with a high self-resonant frequency between power and ground must be used.
   - Note that ferrite material, beads, and filters provide excellent attenuation of ESD currents, in addition to enhancing suppression of radiated emissions.

   For circuit layout (6.4.2):
   - Use a multilayer stackup. Multilayer PCBs are superior to single- and double-sided assemblies because a stable ground layer is available.
   - Filter critical circuits and lines. It is impossible to ascertain which traces will become susceptible to an ESD event.
   - Keep a low ground impedance connection between multiple PCBs and interconnects.
   - Minimize loop areas; identify areas where loop currents can exist.
   - Tightly control coupling between power and ground. This is accomplished by keeping the power and ground traces physically close together.
   - Use a single-point ground methodology for low-speed, low-technology products.
   - Fill in both top and bottom layers of the PCB with as much copper at ground potential (ground fill) as possible.
   - Implement moating and isolation between ESD-sensitive components from other functional areas.
   - When a multilayer PCB is provided, guarantee that a ground plane surrounds every plated through-hole.
   - Physically connect transient protection devices to chassis ground, not circuit or system ground. ESD events contain large amounts of current.
   - Keep routed trace lengths as short as possible.
   - Keep signal lines as close as possible to ground lines, ground planes, and circuits.

   For system-level protection (6.4.2):
   - Provide a complete shield around components and circuits sensitive to radiated ESD corruption. Route internal cables away from slots and openings.
   - Protect all I/O cable entries with suppressors: resistors, *RC* network, *LC* filter, capacitor to ground, ferrite beads, diodes, or similar components.
   - Make all chassis ground connections low impedance. Locate these ground connections at positions where they will conduct ESD impulse energy away from sensitive circuits rather than through them.
   - When membrane keypads for user control are provided, recess the conductive layer of the membrane to eliminate direct discharge to digital circuits directly to the enclosure shield and around the entire perimeter, even when a relatively low-conductivity material is provided.
   - Use metal housings for connector backshells. An ESD event to a connector backshell can cause serious damage, as capacitive

coupling of the energy will occur to the internal wires or to circuits internal to the system.
- Avoid pigtails. Pigtails present problems for both EMI and ESD.

8. Install a guard band (both top and bottom layers) around the periphery of the board to prevent ESD coupling into logic areas due to handling of the board (6.5).
   - Connect the guard band to chassis ground every 1/2 in. (0.5 mm) along the perimeter. This provides a low-impedance path for ESD energy to dissipate to. Do not use solder mask on the guard band.
   - Do not incorporate the guard band as a complete circle around all edges sides of the PCB. Ensure that a break is provided within the band to prevent the band from becoming a loop antenna.

[1]Tranzorb is a trademark of General Semiconductor.

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CHAPTER 7: —BACKPLANES, RIBBON CABLES, AND DAUGHTER CARDS

1. Proper pin assignment will maintain ground loop control. A large number of ground pins help prevent crosstalk, maintain impedance control, reduce radiated emissions, and provide for enhanced signal quality performance (7.1).

2. A constant impedance must be maintained for all traces throughout the interconnect assembly from source to load. The impedance of the connector must be considered at all times (7.1).

3. It is important to calculate and maintain proper impedance for all connector pins. Impedance changes in the trace route will affect the signal integrity of the system, in addition to consuming additional drive current from the power supply (7.1).

4. Impedance-controlled connectors should be used where possible (7.1).

5. When selecting a pinout assignment within an interconnect, remember the following (7.2):
   - When ground pins are assigned, minimize ground loop areas to prevent high-amplitude levels of RF currents from being coupled to other components or subsystems.
   - When designing interconnects, give consideration to all clock and/or periodic signal traces. A clock trace *must always have an adjacent RF return path on all sides of the connector or interface*.
   - Design backplanes with alternating signal and ground traces when using the same routing layer. Use as many ground traces as possible. Do not bunch RF return ground to a single set of multiple pins at one end of the connector. Large RF loop currents will be developed in addition to possible crosstalk between adjacent traces.
   - Place a ground or RF return trace adjacent to, and around, all clock traces.

6. For AC chassis planes (7.3):
   - Some applications require use of an AC chassis plane in addition to 0V-reference planes. This AC chassis plane has no direct connection to other reference planes except through bypass capacitors (usually 0.1 μF). The AC chassis plane must, however, be located directly next to a 0V-reference plane, providing very tight capacitive coupling between the two planes thus minimizing use of discrete capacitors.
   - Power return planes (either DC or AC) may be connected to the AC chassis plane (chassis) if the logic circuitry permits for this type of grounding implementation.
   - When using a chassis plane, the digital logic power and return plane must be electrically isolated at low frequencies from chassis potential.

7. When defining a backplane or interconnect assembly, five areas of concern exist (7.4):
   - Purity of the power distribution system from noise-induced voltage and high-frequency RF currents injected into the planes.
   - Signal quality of the bus that contains parallel traces (crosstalk

concern).
   - Impedance control and capacitive loading for each trace route.
   - Interboard coupling of RF currents (radiated coupling between two boards).
   - Field transfer coupling of daughter cards to card cage (daughter card corrupting its plug-in module).
   - To prevent RF coupling between parallel assemblies, provide for a shield partition between the two PCBs. This shield partition must be securely fastened to the PCB in as many locations as possible.

8. Proper referencing of the backplane to the card cage requires establishing a very low-impedance RF reference between the backplane and card cage. This reference method is mandatory to short out eddy currents developed at and by the daughter cards (7.4).
   - To be reasonably effective, the RF transfer impedance between the logic return planes and AC chassis plane must be equal to, or less than, 1-Ω, thereby shorting out common-mode potential between daughter card and backplane.
   - Enhanced EMI and system performance will be gained when the signal impedances on the routing layers are well controlled and preferably referenced to the ground planes rather than voltage planes.
   - An image plane must be located adjacent to each and every signal plane. Bond the ground planes together in as many locations as possible with vias.
   - It must be determined whether the top layer of the backplane is to be a ground plane or a signal plane. Making this top layer a ground plane minimizes the impedance mismatch presented between the backplane and I/O connectors.
   - If the top and bottom layers of the backplane, or daughter card, is a solid plane at 0V-reference or ground potential, a low-impedance connection to *chassis* ground becomes available to both the backplane connector and the faceplate screw securement.

9. When using many connector slots, a worst case analysis must be performed to determine waveform degradation due to lumped distributed capacitance. Always provide for sufficient grounding of the backplane in multiple locations. Include in the measurement all adapter cards that plug into the backplane (7.4.1).

10. With many connector slots, there will be a larger value of lumped distributed capacitance presented to the circuit. With additional capacitance, degradation of signal quality can occur, sometimes to the point of nonfunctionality (7.5).

11. The interface connectors chosen must be appropriate for the edge rate transition of the desired signal, along with proper impedance matching between backplane and adapter cards (7.5).

12. Design techniques for interconnects using parallel routed traces include (7.5)
   - Keeping discontinuities as short as possible.
   - Using as many ground connections as possible within the allocated space or pinout.
   - Establishing a common ground reference within the connector.
   - Using low dielectric constant board materials.
   - Maintaining the RF return path as close as possible to the signal path.

13. During layout, sufficient real estate must be present to apply filtering and termination for both signal traces and I/O interconnects (7.6).

14. Vias must be avoided when routing signal traces between planes for high-threat signals. High-threat signals are defined as reset, clock, audio, video, analog, high-speed transmission of data, and related signals. Each via adds approximately 1–3 nH inductance and 2 pF to the trace route (7.7).

15. T-stubs must not be used in a trace route (7.7).

16. Trace routing must be as short as possible to prevent ringing and reflections that may occur on electrically long traces (7.8).

17. All clock traces must be terminated in their characteristic impedance. The terminating resistor must be the last item on the bus. The slowest speed logic possible must be used (7.8).

18. The main concern with crosstalk, related to parallel traces, is to prevent electrical noise on one trace (source trace) from causing harmful interference to a victim trace (7.9).

19. To minimize crosstalk between traces and planes, the *3-W rule* or separate parallel traces is required (7.9).

20. Three types of signal transmission configurations exist when crossing a boundary. These are (7.9):
    - A one 0V-reference trace adjacent to each signal trace.
    - A ground plane or RF return path adjacent to all signal traces in the assembly.
    - Use twisted pair ribbon cable.

21. When using interconnects for backplanes, ribbon cables, or adapter cards, the optimal arrangement is to alternate the transmission path traces between signal and 0V-reference, or ground (7.9).

22. Use of a shield partition is desired when several ribbon cables are stacked against each other. Long cable routes allow crosstalk to be developed (7.9).

23. For signal pair routing, twisting the traces using an even number of twists enhances signal integrity. This is extremely difficult and generally not practical to implement. This technique is currently outdated and rarely used in high-technology products (7.9).

24. For one or two layer backplanes, a ground trace must be routed parallel to each signal trace pair (7.10).

25. Signal traces must not be routed across through-hole connector pins that overlap each other. This routing method prevents the image planes from providing a low-impedance path for RF return currents. Return currents must travel around the long edge of the I/O connector to complete its path, thus maximizing generation of RF common-mode noise (7.11).

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CHAPTER 8: —ADDITIONAL DESIGN TECHNIQUES

Localized Planes (8.1)

1. During component placement, oscillators, crystals, and support circuitry (buffers, drivers, etc.) must be located over a single localized plane. This plane is usually at ground potential, but *can* be at voltage potential. Locate clock generation circuits near a ground stitch location.

2. When using localized planes, the following must be observed:
   - Locate clock circuitry and localized plane next to an adjacent ground stitch location and bond the localized plane to chassis ground, if ground is the chosen potential.
   - In addition, connect the localized ground plane, if ground is the chosen potential, to the main 0V-reference plane using vias.
   - Include support circuitry, drivers, buffers, and resistors in this localized plane area.

3. A unique benefit of localized planes is the ability to develop, at no cost, additional decoupling for specific components. A capacitor, by definition, is two parallel plates separated by a dielectric. Because a localized plane is incorporated on the outer layer of the PCB, directly under a component, the ability to add more decoupling into the artwork is a simple matter of implementation.

20-H Rule (8.2)

1. RF current will radiate off edges of the PCB as a result of interplane coupling between the power and ground planes due to magnetic flux linkage. This interplane coupling is called *fringing* and is generally observed on only very high-speed PCBs.

2. All power planes should be made physically smaller than their respective ground planes per the *20-H rule*. This rule is not required for every PCB. Take into consideration the physical size of the PCB related to $\lambda/20$ of the highest generated frequency on the PCB.

3. When using the *20-H rule*, any traces on the adjacent signal routing plane, located over the absence of copper area, must be rerouted inward to be physically adjacent to a solid reference plane (voltage or ground), with no exceptions allowed.

4. If functional partitioning is required on the PCB, *20-H* should be implemented in high-frequency bandwidth areas only (CPU, video, Ethernet, SCSI, LAN interfaces, and other high-speed circuits).

Trace Routing for Corners (8.3)

1. Contrary to past beliefs, 90-degree corners do not affect the performance of a PCB layout! The impedance of the transmission line will, however, be lower at each corner. The magnitude of this impedance change is approximately 10% but for only 17 ps. Because an electromagnetic field propagates at approximately 60% the speed of light, only signals that exceed 33 GHz will be affected by this impedance discontinuity. Once we exceed 1 GHz, different design and layout techniques are required anyway.

2. Right-angle corners radiate RF energy. The *magnitude* of emissions is approximately 3 to 5 dB, which is so small that most instrumentation cannot measure it! Components that drive the transmission line generate thousands of times more magnitude of RF energy. Therefore, right-angle corners have no or minimal impact related to EMI emissions when routed microstrip. Radiated effects from stripline do not exist, since traces routed internal to the PCB cannot radiate to the outside environment.

3. The main reason for not designing a PCB with right-angle corners lies with manufacturing. When traces are etched, the chemicals start at the corners. During the etching cycle, the corner will be etched back a certain amount, thus causing the physical dimension to decrease. This smaller trace width may not be able to carry current and can self-destruct under maximum load conditions. Vendors thus cannot manufacture a PCB with right-angle corners.

Selecting Ferrite Components (8.4)

1. There are three common ways to select ferrites for suppression of unwanted signals, from least used to most for a particular application:
   - Used as a shield to isolate a conductor, component, or circuit from stray electromagnetic fields.
   - When used with a capacitor, to create a low-pass filter that is inductive-capacitive at low frequencies and dissipative at higher frequencies.
   - To prevent parasitic oscillation or to attenuate unwanted signal coupling traveling along component leads, interconnecting wires, traces, or cables. When used as a lossy element, ferrites remove or absorb electromagnetic energy present within a transmission line.

2. When selecting a ferrite device for suppression of RF energy, consider the following:
   - Select a material based on the impedance presented to the circuit.
   - Determine the permeability value for the optimal frequency range of operation.
   - Alter the core size, shape, or length to change the impedance value.
   - Elevated temperatures will decrease overall impedance and performance.
   - Extreme bias (current flow through the material), decreases the impedance to the point of nonfunctionality.
   - Determine if AC or DC current is passed through the device. Excessive attenuation of a "wanted" signal could occur.
   - To increase the impedance of shield beads or cores, add more turns of wire. However, the spectral bandwidth of performance is decreased.

Grounded Heatsinks (8.5)

1. On high-speed VLSI processors (generally 100 MHz and above), a grounded heatsink may be required.

2. Heatsinks must be bonded to the ground planes or 0V-reference by a metallic connection. Use of a fence (similar to a vertical bus bar) from the PCB to the heatsink will encapsulate the processor. This fence also allows for a Faraday shield to be present around the processor, thus preventing common-mode noise RF energy internal to the package from radiating into free space or from coupling onto nearby components, cables, peripherals or into aperture slots.

3. This heatsink is generally used in conjunction with differential-mode decoupling capacitors located on the top of the components' ceramic package, if provisions are available for top-mounted capacitors.

4. The heatsink is connected to the ground plane(s) through a mounting fence or bracket.

5. The heatsinks' ground posts are decoupled with alternate sets of parallel decoupling capacitors around all four sides of the processor.

6. A dielectric material is selected for thermal conduction of heat. This material may also be used to determine the resonant frequency of the heatsink assembly. This resonance is used as part of a *common-mode* decoupling capacitor that shunts RF energy away from the silicon wafer (voltage potential) to ground (ground potential).

7. To summarize, a grounded heatsink creates
   - A thermal device to remove heat generated internal to the package.
   - A Faraday shield to prevent RF energy from clock circuitry internal to the processor from radiating into free space or corrupting adjacent components.
   - A *common-mode* decoupling capacitor that removes common-mode RF currents directly from the die, inside the package, by AC coupling RF energy to ground.

Lithium Battery Circuits (8.6)

1. International safety agencies require protection against explosion from lithium batteries should an abnormal fault occur-short circuit or reverse bias during a charging cycle.

2. This protection must be redundant in nature, consisting of two diodes back to back or a diode and a resistor in series per product safety requirements. This includes discrete batteries, NVRAMs, clock calendars, and similar energy storage circuits.

BNC Connectors (8.7)

1. BNC connectors require special considerations when incorporated on a PCB. For interconnects, where the braid of the coax is required for RF shielding, the shell of the connector must be bonded to chassis ground at the bulkhead, or I/O panel through a low-impedance path to the 0V-reference.

2. For applications where the shell of the BNC connector is *signal return* and is not used as a *RF return shield*, the shell of the BNC connector must be connected through a low-impedance path to the 0V-reference of the signal return circuit. *Do not* connect the ground (outer barrel) pin of the BNC connector to the I/O isolated (quiet ground) area.

3. If using an isolated BNC connector, the shell or shield of the connector must not be bonded to chassis ground. The base of the connector is isolated using a nonconductive bushing (insulator) or equivalent means.

4. Pigtails are not to be used under any condition to connect the shell or ground pin of the BNC connector to chassis ground or to any other ground in the system, unless system functionality mandates this ground connection.

Creepage and Clearance Distances (8.8)

1. Safety agencies are concerned with the potential risk of electric shock that may occur between traces and conductive parts of a system.

2. The definition for creepage and clearance, defined by harmonized safety standards, is:
   - Creepage is the shortest path between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured along the surface of the insulation.
   - Clearance is the shortest distance between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured through air.
   - Bounding surface is the outer surface of the electrical enclosure considered as though metal foil was pressed into contact with the accessible surface of insulation material.

Current-Carrying Capacity of Copper Traces (8.9)

The power-handling capability of copper traces is based on cross-sectional area, related to temperature rise. For a specific cross-sectional area, the temperature rise within a trace, above ambient levels, is approximately proportional to the power dissipated in the trace. An excessively large temperature rise makes circuits unreliable, heats up the dielectric material, and may cause destruction of the trace. To be conservative during the design cycle, an upper limit on the heating of traces should not exceed 10° C above ambient.

Film and Manufacturing Issues (8.10)

1. Because of the increasing density, the manufacturing process needs to be monitored closely. Concerns include:
   - *Test Coupons*. Test coupons allow for easy measurement of the actual impedance of the signal planes.
   - *Layer Stackup Window*. Etched onto each layer is a number, in a box, that reflects the identity of a layer internal to the board stackup.
   - *Stacking Stripes*. Stacking stripes is a technique in which copper from all layers is routed to the outside edge of the PCB to determine the actual width of traces after etching.
   - *Test Points*. Test points are used to help analyze whether a broken trace or faulty component exists within the manufactured product; they allow for ease of debugging a fully assembled PCB.
2. All unconnected vias must be removed from the artwork prior to production of the film.
3. For compliance with product safety standards, use of flame-retardant material for the fiberglass assembly material is mandatory.

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Appendix B - International EMC Requirements

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Appendix B: International EMC Requirements

BRIEF SUMMARY OF NORTH AMERICAN EMC REQUIREMENTS

Electrical and electronic products generate RF energy. Emission levels are set by rules and regulations mandated by both domestic and international governments or agencies. In the United States, the Federal Communications Commission (FCC) regulates the use of radio and wire communications. The FCC, an independent government agency reporting to the Congress of the United States, is responsible for ensuring interstate and international communication by radio, television, satellite, and cable.

In Canada, Industry Canada (IC) is the agency responsible for regulating radio and wire communication. Industry Canada performs the same function as the Federal Communications Commission. Harmonized test requirements and standards for North America have been developed between the two countries.

The FCC defines a digital device as:

> An unintentional radiator (device or system) that generates and uses timing signal or pulses at a rate in excess of 9,000 pulses (cycles) per second and uses digital techniques; inclusive of telephone equipment that uses digital techniques or any device or system that generates and uses radio frequency energy for the purpose of performing data processing functions, such as electronic computations, operations, transformation, recording, filing, sorting, storage, retrieval or transfer.

Digital computing products are classified into two categories: Class A and B. The FCC and Industry Canada use the same definition.

Class A:

> A digital device that is marketed for use in a commercial, industrial, or business environment, exclusive of a device which is marketed for use by the general public or is intended to be used in the home.

Class B:

> A digital device that is marketed for use in a residential environment, notwithstanding its use in a commercial, industrial, or business environment. Examples of such devices include, but are not limited to, personal computers, calculators, and similar electronic devices that are marketed for use by the general public.

If a product contains digital circuitry and has a clock frequency greater than 9 kHz, it is defined as a digital device and is subject to the rules and regulations of the FCC. Electromagnetic Interference (EMI) may occur as a result of both time domain and frequency domain components of digital and analog circuits. These products are subject to domestic and international regulatory requirements.

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BRIEF SUMMARY OF WORLDWIDE EMC REQUIREMENTS

Two routes to compliance are available: self-certification and Technical Construction File (TCF). Self-certification is the preferred route because of its simplicity and faster time to market. This route depends on the availability of test standards that have been published in the *Official Journal of the European Union* (*OJ*), applicable to the product to be evaluated. In many cases, a specific product category may not exist.

When a specific standard does not exist, or it is not possible to test all the possible configurations because of a large number of variants, alternate construction features, user options, and the like, a Technical Construction File (TCF) may be a better choice. The caveat is that if use of a TCF is required, mandatory assessment and approval must be issued by a European Competent Body, certified by a European National Authority. A National Authority is authorized by a country's government to oversee the licensing of Competent Bodies and Notified Bodies. Notified Bodies were established to issue approvals for telecommunication equipment. Competent Bodies assess products to the EMC Directive and various product safety directives. A Competent Body is issued a license to grant approval to a particular range and type of product that they are considered technologically knowledgeable to assess. Assessment must occur within mainland Europe. Competent Bodies may, however, own and operate field offices around the world.

Three tiers of standards are detailed in the EMC Directive: basic, generic, and product family.

Basic Standards

Basic standards are referenced within generic and product family standards as a basis for performing a particular test. The standards include most IEC and CISPR standards. These standards are dedicated to aspects of EMC that are of general interest to all committees working on, creating, or developing other standards. This development work includes product family standards. It is common for a product family standard to take the appearance of a generic standard. Specific operational modes and configurations are detailed, including performance criteria and test levels.

Generic Standards

Generic standards were developed for industry sectors for which no product family standard is available. Generic standards encompass all environments and applications, and are intended to represent the essential requirements of a directive. These standards are divided into two basic requirements: emissions and immunity. Environment is defined as residential, commercial, light industrial, or heavy industrial.

When a relevant product family standard is not available, generic standards take precedece. Regarding product categories, a particular device might have a product family emissions standard, and yet be required to use a generic standard for immunity tests. The reason for this is that specific test requirements for immunity may be in the development stage or not yet published in the *OJ*.

Generic Standards (Sample List)

Part 1:Residential, Commercial, and Light Industry

EN 50081-1	Electromagnetic compatibility—Generic emission standard.
EN 50082-1	Electromagnetic compatibility—Generic immunity standard.

Part 2:Industrial Environment

EN 50081-2	Electromagnetic compatibility—Generic emission standard.
EN 50082-2	Electromagnetic compatibility—Generic immunity standard.

Part 3:Special Environment

EN 50081-3	Electromagnetic compatibility—Generic emission standard.
EN 50082-3	Electromagnetic compatibility—Generic immunity standard.

Product Family Standards

Product family standards take precedence over generic and basic standards after they are published in the *Official Journal of the European Union*. These standards may be specifically designed to cover a particular aspect of EMC for a particular product, or product family, such as Information Technology Equipment (ITE) or Industrial, Scientific and Medical Equipment (ISM). In addition, product family standards may be created as an addendum to existing product performance standards.

Product family standards refer to internationally adopted basic standards, such as the IEC 1000-4-X series for immunity test requirements. These requirements define what tests are to be performed, test levels or limits, operational conditions, and performance criteria. Product family standards are generally based on input from professional engineers and companies that specialize within a particular industry. Companies have a more comprehensive concept of the EMC environment than that of a technical committee. Working together, industrial and technical committees are best suited to developing realistic test procedures and methodologies to meet the essential requirements of the EMC directive.

International Definition, Defined within EN 55022 and CISPR-22

Products are classified into two categories for emissions: Class A and B. The definition provided by CISPR 22, which is identical to EN 55022 for information technology equipment (ITE), follows. (Most products described within this book fall within this definition.[1])

Class A ITE:

> Class A ITE is a category of all other ITE which satisfies the Class A ITE limits but not the Class B ITE limits. Such equipment should not be restricted in its sale but the following warning shall be included in the instructions for use:
>
> **Warning** This is a Class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

Class B ITE:

> Class B ITE is a category of apparatus, which satisfies the Class B ITE disturbance limits. Class B ITE is intended primarily for use in the domestic environment and may include

- equipment with no fixed place of use; for example, portable equipment powered by built-in batteries;
- telecommunication terminal equipment powered by a telecommunication network;
- personal computers and auxiliary connected equipment.

Note The domestic environment is an environment where the use of broadcast radio and television receivers may be expected within a distance of 10 m of the apparatus concerned.

[1] EN 55022:1995 (CISPR 22:1993). Limits and methods of measurement of radio disturbance characteristics of information technology equipment.

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FCC/ INDUSTRY CANADA EMISSION LIMITS

For FCC and Industry Canada, the frequency range to be measured is based on the highest fundamental internally generated clock frequency per the following list:

Less than 1.705 MHz	Test to 30 MHz
From 1.705 MHz to 108 MHz	Test to 1 GHz
108 MHz to 500 MHz	Test to 2 GHz
500 MHz to 1 GHz	Test to 5 GHz
Above 1 GHz	Test to 5th harmonic or to 40 GHz, whichever is lower

FCC/DOC Class A Conducted Emission Limits

Open table as spreadsheet

Frequency	Quasi-Peak Limit
0.45 to 1.705 MHz	60.0 dBµV
1.705 to 30.0 MHz	69.5 dBµV

FCC/DOC Class B Conducted Emission Limits

Open table as spreadsheet

Frequency	Quasi-Peak Limit
0.45 to 30.0 MHz	48.0 dBµV

FCC/DOC Class A Radiated Emission Limits

Open table as spreadsheet

Frequency (MHz)	Distance (meters)	Quasi-Peak Limit (dBµV/m)
30 to 88	10	39.0
88 to 216	10	43.5
216 to 960	10	46.5
Above 960	10	49.5

FCC/DOC Class B Radiated Emission Limits

Open table as spreadsheet

Frequency (MHz)	Distance (meters)	Quasi-Peak Limit (dBµV/m)
30 to 88	3	40.0
88 to 216	3	43.5
216 to 960	3	46.0
Above 960	3	54.0

International Emissions Limits Summary—Sample List

The following list deals with emission requirements for the European Union. These standards are identified as product family standards.

Product Family Standards (Sample List)

EN 55011	Limits and methods of measurements of radio disturbance characeristics of industrial, scientific, and medical (ISM) radio frequency equipment (CISPR 11).
EN 55013	Limits and methods of measurements of radio disturbance characteristics of broadcast receivers and associated equipment (CISPR 13).
EN 55014	Limits and methods of measurements of radio disturbance characteristics of household electrical appliances, portable tools, and similar electrical apparatus (CISPR 14).
EN 55022	Limits and methods of measurements of radio disturbance characteristics of information technology equipment (CISPR 22).
EN61000-3-2	Harmonic Current Emissions.
EN61000-3-3	Voltage Fluctuations and Flicker in low-voltage supply systems.

Class B Limits for Light Industrial Equipment and Primarily Residential Areas

Open table as spreadsheet

Frequency Range, MHz									
0.15 ---------- 0.5 ---------- 5 ---------- 30 ---------- 230 ---------- 1000									
SPECIFICATION	**dBµV**		**dBµV**		**dBµV**		**dBµV/m**	**dBµV/m**	**NOTES**
	QP (1)	**AVG (1)**	**QP**	**AVG**	**QP**	**AVG**	**QP (1)**	**QP**	
EN 55011 (Group 1)	66-56	56-46	56	46	60	50	30	37	@ 10 m, B limit
EN 55013 (2)	66-56	56-46	56	46	60	50	45–55 (3)	—	dBpW, Absorbing Clamp (3)
EN 55014	66-56	56-46	56	46	60	50	45–55 (3)	—	dBpW, Absorbing Clamp (3)
EN 55022	66-56	56-46	56	46	60	50	30	37	@ 10 m
Class A Limits for Industrial Areas									
EN 55011 (Group 1)	79	66	73	60	73	60	30	37	@ 30 m, A limit
EN 55022	79	66	79	66	73	60	30/40	37/47	@ 30 m/10 m

Note (1) The dash between two numbers (e.g., 66-56) means that the limit decreases with the logarithm of frequency.

(2) EN 55013 has other limits for emissions from receivers and televisions.

(3) Absorbing clamp measurement is for the frequency range of 30–300 MHz only.

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EMISSIONS—EN 55011 INDUSTRIAL SCIENTIFIC AND MEDICAL (ISM) EQUIPMENT

For all other EN 55 XXX specifications, refer to the International Emissions Limits Summary.

Special Note: *Because of the unique specification limits for EN 55011, this section is provided for completeness only*.

Classification of ISM Equipment

Group 1 ISM—Group 1 contains all ISM equipment in which there is intentionally generated and/or used conductively coupled radio frequency energy that is necessary for the internal functioning of the equipment itself.

Group 2 ISM—Group 2 contains all ISM equipment in which radio frequency energy is intentionally generated and/or used in the form of electromagnetic radiation for the treatment of material and spark erosion equipment.

Line Conducted Emissions

Emissions levels less than Class A limits (Table IIA), or as agreed with the competent body. The need for mains terminal disturbance voltage limit for Class A equipment *in-situ* is under consideration.

Table IIA: Mains terminal disturbance limits for Class A equipment measured on a test site

➡ Open table as spreadsheet

Class A Equipment Limits dB(μV)				
	Group 1		Group 2[a]	
Frequency band (MHz)	Quasi-peak	Average	Quasi-peak	Average
0.15–0.50	79	66	100	90
0.50–5	73	60	86	76
5–30	73	60	90	80
			Decreasing with logarithm of frequency to 70	Decreasing with logarithm of frequency to 60

[a] Mains terminal disturbance voltage limits for Group 2, Class A equipment requiring input current greater than 100A are under consideration.

Table IIB: Mains terminal disturbance limits for Class B equipment measured on a test site

➡ Open table as spreadsheet

Class B Equipment Limits dB(μV)

	Groups 1 and 2	
Frequency Band (MHz)	**Quasi-peak**	**Average**
0.15–0.50	66 Decreasing with logarithm of frequency to 56	56 Decreasing with logarithm of frequency to 46
0.50–5	56	46
5–30	60	50

Table III: Electromagnetic radiation disturbance limits for Group 1 equipment

Open table as spreadsheet

	Measured on a test site		Measured in situ
Frequency Band MHz	Group 1, Class A 30 m measurement distance dB(µV/m)	Group 1, Class B 10 m measurement distance dB(µV/m)	Group 1, Class A limits with measuring distance 30 m from exterior wall outside the building in which the equipment is situated dB(µV/m)
0.15–30 30–230 230–1000	Under consideration 30 37	Under consideration 30 37	Under consideration 30 37

Table IV: Electromagnetic radiation disturbance limits for Group 2, Class B equipment measured on a test site

Open table as spreadsheet

Frequency band	**Class B limits measurement distance 10 m**
MHz	**dB(µV/m)**
0.15–30	Under consideration
30–80.872	30
80.872–81.848	50
81.848–134.786	30
134.786–136.414	50
136.414–230	30
230–1000	37

Table V: Electromagnetic radiation disturbance limits for Group 2, Class A equipment

Open table as spreadsheet

	Limits with Measuring Distance 30 m	
Frequency Range (MHz)	**From exterior wall outside the building in which the equipment is situated dB(µV/m)**	**On a test site dB (µV/m)**
0.15–0.49	75	85
0.49–1.705	65	75
1.705–2.194	70	80
2.194–3.95	65	75
3.95–20	50	60
20–30	40	50

30–47	48	58
47–68	30	40
68–80.872	43	53
80.872–81.848	58	68
81.848–87	43	53
87–134.786	40	50
134.786–136.414	50	60
136.414–156	40	50
156–174	54	64
174–188.7	30	40
188.7–190.979	40	50
190.979–230	30	40
230–400	40	50
400–470	43	53
470–1000	40	50

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SUMMARY OF CURRENT INTERNATIONAL IMMUNITY REQUIREMENTS

To be able to certify compliance to the EMC Directive, 89/336/EEC, manufacturers must construct products that meet not only emissions requirements, but also immunity levels, or protection against harmful disruption from other electronic equipment. Currently, only Europe requires immunity testing. Since the IEC and CISPR are international organizations, the scope of their work is implememted throughout the world. CENELEC adopts basic standards developed by both IEC and CISPR, and publishes them as harmonized standards to meet the EMC Directive. The European harmonized document and IEC publication numbers are similar. The IEC standard is prefixed with IEC 1000-4-X. When referenced as a European harmonized document, this number is changed to EN 61000-4-X.

IEC standards for immunity are provided in the IEC 1000-4-X series. This series of standards describes the test and measurement methods detailed within the basic standards. Basic standards are specific to a particular type of EMI phenomenon, not a specific type of product. This series covers the following:

- Terminology.
- Descriptions of the EMI phenomenon.
- Instrumentation.
- Measurement and test methods.
- Ranges of severity levels with regard to the immunity of the equipment.

The most commonly used immunity standards adopted or recommended by CENELEC, the international IEC 1000-X series of standards were reissued using an EN 61000-X specification number. The EN 61000-4-X series of immunity specifications are as follows:

Comprehensive List of Immunity Standards

Standard	Description
EN 61000-4-2	Electrostatic discharge (ESD)
EN 61000-4-3	Radiated electromagnetic field
EN 61000-4-4	Electrical Fast Transient (EFT)/Burst
EN 61000-4-5	Surge
EN 61000-4-6	Conducted disturbance by RF fields
EN 61000-4-7	General guide on harmonics and interharmonics measurements and instrumentation (not a standard; procedure only)
EN 61000-4-8	50/60 Hz magnetic field
EN 61000-4-9	Pulsed magnetic field
EN 61000-4-10	Oscillatory magnetic field
EN 61000-4-11	Voltage dips and interruption
EN 61000-4-12	Oscillatory waves "ring wave"
EN 61000-4-13	Oscillatory waves 1 MHz
EN 61000-4-14	Harmonics, interharmonics, and main signaling
EN 61000-4-15	Voltage fluctuations
EN 61000-4-27	Unbalance in three-phase mains
EN 61000-4-28	Variation of power frequency

Note Several EN 61000-4-x specifications have never been written or released. Titles have been issued and working groups assigned. When performing compliance testing, verify which standards are mandatory for your product along with required test levels and performance criteria.

Performance Criteria for Immunity Tests

A functional description and a definition of performance criteria, during or as a consequence of EMC testing, shall be provided by the manufacturer and noted in a test report based on the following criteria:

PERFORMANCE CRITERION A: The apparatus *shall continue to operate as intended*. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer when the apparatus is used as intended. In some cases, the performance level may be replaced by a permissible loss of performance. If the minimum performance level or the permissible performance loss is not specified by the manufacturer, then either of these may be derived from the product description and documentation (including leaflets and advertising) and what the user may reasonably expect from the apparatus if used as intended.

PERFORMANCE CRITERION B: The apparatus *shall continue to operate as intended after the test*. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer when the apparatus is used as intended. In some cases, the performance level may be replaced by a permissible loss of performance. During the test, degradation of performance is, however, allowed. No change of actual operating state or stored data is allowed. If the minimum performance level or the permissible performance loss is not specified by the manufacturer, then either of these may be derived from the product description and documentation (including leaflets and advertising) and what the user may reasonable expect from the apparatus if used as intended.

PERFORMANCE CRITERION C: Temporary loss of function is allowed, provided the loss of function is self-recoverable or can be restored by the operation of the controls.

International Immunity Requirements for Selected Products

➡ Open table as spreadsheet

SPECIFICATION	EN 61000-4-2 Electrostatic Discharge	EN 61000-4-3 Radiated RF Immunity	ENV 50204 Radiated RF Immunity	EN 61000-4-4 Electrical Fast Transients	EN 61000-4-5 Transients Signal Leads	
EN 50082-1	8 kV (Air)	80–1000 MHz	900 ± 5 MHz	500 V, Signal	1.2/50µs	
Generic limit	4 kV (Direct)	3 V/m	Pulse modulated	500 V, DC power	AC power:	1kV-CM
light industrial equipment[a]		1 kHz, 80% AM	50% duty cycle	500 V, Process		500V-DM
			200 Hz	1,000 V, Power	DC power:	500V-CM
				5/50 ns, 5 kHz		500V-DM
					Process:	500V-CM
	Criteria B	Criteria A	Criteria A	Criteria B	Criteria B	
EN 50082-2	8 kV (Air)	10 V/m	900 ± 5 MHz	1,000 V, Signal	1.2/50µs	
Generic limit	4 kV (Direct)	1 kHz, 80% AM	Pulse modulated	2,000 V, Power	AC power:	4 kV-CM
Heavy industrial equipment[b]		80–1000 MHz	50% duty cycle	5/50 ns, 5 kHz	2 kV-DM	
		except 3 V/m at	200 Hz		DC power:	500V-CM
		87–108 MHz				500V-DM
		174–230 MHz			Process:	2 kV-CM
		470–790 MHz				1 kV-DM
	Criteria B	Criteria A	Criteria A	Criteria B	Criteria B	
EN 55014-2	8 kV (Air)	80–1000 MHz	Not yet proposed	500 V, Signal	1,000 V, DM	
Appliances and power tools	4 kV (Direct)	3 V/m		1000 V, AC	2,000 V, CM on power only	
				5/50 ns, 5 kHz	1.2/50 µs	
	Criteria B	Criteria A		Criteria B	Criteria B	
EN 60601-2	8 kV (Air)	26–1,000 MHz	Not yet proposed	500 V, Signal-/I/O	1,000 V, DM	
Medical devices	3 kV (Direct)	3 V/m, 80% AM−1 kHz		1,000 V, AC	2,000 V, CM	
					5/50 ns, 5 kHz 1.2/50 µs power lines only	
	Criteria B	Criteria A		Criteria B	Criteria B	

[a] Severity levels and frequency ranges are subject to change. Consult test requirements for current values in effect at date of testing and certification.

[b] Additional test requirements exist but are not detailed above. Refer to EN 55082-2 for details.

[c]Severity levels and frequency ranges are subject to change. Consult test requirements for current values in effect at date of testing and certification.

[d]Additional test requirements exist but are not detailed above. Refer to EN 50082-2 for details.

CM: Common-mode

DM: Differential-mode

Performance criterion

Level A: The apparatus shall continue to operate as intended. No degradation of performance or loss of function is allowed.

Level B: The apparatus shall continue to operate as intended after the test.

Level C: Temporary loss of function is allowed, provided the loss of function is self-recoverable.

Open table as spreadsheet

SPECIFICATION	EN 61000-4-6 Conducted RF Immunity	EN 61000-4-8 Radiated Magnetic	EN 61000-4-11 Voltage Dips, Interruption, Variation	EN 61000-3-2 Power Line Harmonics	EN 61000-3-3 Flicker
EN 50082-1	0.15-80 MHz	3 A/m	+10%, −15% (A)	Required for specific products.	Required for specific products.
Generic limit	3 V	50 Hz	−30%, 10ms (B)	Consult standard for test details.	Consult standard for test details.
light industrial equipment[c]	1 kHz		−60% ,100ms (C)	(Emissions requirement)	(Emissions requirement)
	80% AM,		−95%, 5000ms (C)		
	150 Ω Source				
	Criteria A	Criteria A	Criteria (x) above		
EN 50082-2	0.15–80 MHz	30 A/m	+10%, −15% (A)	Not required	Not required
Generic limit	10 V	50 Hz	−30%, 10ms (B)		
heavy industrial equipment[d]	80% AM,		−60% ,100ms (C)		
	1 kHz		−95%, 5000ms (C)		
	150 Ω Source				
	Criteria A	Criteria A	Criteria (x) above		
EN 55014-2	0.15–230 MHz	Not yet proposed	Not yet proposed	Not yet proposed	Not yet proposed
Appliances and power tools	Category II				
	0.15–80 MHz				
	Category IV				
	1 V, Signal				
	3 V, Power				
	Criteria A				
EN 60601-2	Not yet proposed	Not yet proposed	Not yet proposed	Not yet proposed	Not yet proposed
Medical devices					

[a]Severity levels and frequency ranges are subject to change. Consult test requirements for current values in effect at date of testing and certification.

[b]Additional test requirements exist but are not detailed above. Refer to EN 55082-2 for details.

[c]Severity levels and frequency ranges are subject to change. Consult test requirements for current values in effect at date of testing and certification.

[d]Additional test requirements exist but are not detailed above. Refer to EN 50082-2 for details.

Performance criterion

Level A: The apparatus shall continue to operate as intended. No degradation of performance or loss of function is allowed.

Level B: The apparatus shall continue to operate as intended after the test.

Level C: Temporary loss of function is allowed, provided the loss of function is self-recoverable.

Appendix C - The Decibel

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Appendix C: The Decibel

In the field of engineering, a common unit of measurement or reference is required. This often misunderstood unit, a logarithmic function, is the decibel (dB). It is required because of the scaling range of units involved. Most ratios are dimensionless, whereas some ratios are magnitudes expressed in dB (reference).

The basic unit of measurement is the logarithmic ratio of two products. Absolute power, voltage, or current levels are expressed in dB by giving their value *above* or *referenced* to some base quantity. The following describes power gain ($P2 > P1$) or loss ($P2 < P1$) in a system:

$$\text{Power Gain: } \text{dB} = 10 \log \left(\frac{P_{\text{out}}}{P_{\text{in}}} \right)$$

➪ Get MathML

In many situations, reference must be made for voltage, current, field strength, and the like instead of power. The following describes formulas for voltage and current gain ratios. The unit dB is dimensionless.

$$\text{Voltage gain: } \text{dB} = 10 \log \left(\frac{V_{\text{out}}^2/R}{V_{\text{in}}^2/R} \right) = 10 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right)^2 = 20 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right)$$

$$\text{Current gain: } \text{dB} = 10 \log \left(\frac{I_{\text{out}}^2 R}{I_{\text{in}}^2 R} \right) = 10 \log \left(\frac{I_{\text{out}}}{I_{\text{in}}} \right)^2 = 20 \log \left(\frac{I_{\text{out}}}{I_{\text{in}}} \right)$$

➪ Get MathML

A pattern follows for voltage and current. An exception is the common reference of dB above or below one milliwatt, denoted as dBm. Radiated electromagnetic fields are described in terms of field intensity. These units are V/m (volts per meter) for electric field strength or A/m (amperes per meter) for magnetic field strength. The common units of measurement for the following voltage and current field strength intensity are

$$1\mu\text{V/m} = 0\ \text{dB}\mu\text{V/m}$$
$$1\text{mV/m} = 0\ \text{dBmV/m}$$
$$1\mu\text{A/m} = 0\ \text{dB}\mu\text{A/m}$$

➪ Get MathML

$$1\text{mA/m} = 0\ \text{dBmA/m}$$
$$1\text{mW} = 0\ \text{dBm (Note the pattern difference)}$$

➪ Get MathML

Most regulatory limits are described in μV/m. For example, 100 μV/m limit translates to 40 dBμV/m. The equations that describe this conversion are

$$\text{dB}\mu\text{V/m} = 20 \log_{10} \left(\frac{\text{V/m}}{1\mu\text{V/m}} \right)$$

$$\text{dB}\mu\text{A/m} = 20 \log_{10} \left(\frac{\text{A/m}}{1\mu\text{A/m}} \right)$$

➪ Get MathML

Conversions between units are easy. For example:

1 µV = 0 dBµV = dBm-107 dBm	For a 50 Ω system
V(dBµV) = 90+10log$_{10}$(*Z*)+*P* (dBm)	For a given impedance *Z* in ohms

The proof for this conversion is

0 dBm = 1 mW = 0.001 Watts

$E = \sqrt{mW * R}$ Assume *R* = 50 ohms (*Note:* for dBm, the reference is 1 mW)

$$E = \sqrt{1mW * 50\,\Omega} = 0.224\ V$$

➪ Get MathML

dBµV = 20log$_{10}$ (0.224 *V*/1µ*V*) = 107 dBµV

Therefore, 107 dBµV = 0 dBm in a 50 Ω system

The scale factor is thus: dBm + 107 dB = dbµV

Five commonly used variations exist for the decibel. An example of this variation follows to present the concept of dBs using different units.

$$dBm = 10 \log\left(\frac{P}{0.001W}\right)$$

$$dB\mu V = 20 \log\left(\frac{V}{1\mu Volt}\right)$$

$$dB\mu A = 20 \log\left(\frac{A}{1\mu Amp}\right)$$

$$dB\mu V/m = 20 \log\left(\frac{V}{1\mu Volt/meter}\right)$$

$$dB\mu A/m = 20 \log\left(\frac{V}{1\mu Amp/meter}\right)$$

$$dB\mu V/m/120KHz = 20 \log\left(\frac{A}{1\mu Volt/meter}\right) \text{ at a 120-kHz bandwidth}$$

➪ Get MathML

Several pitfalls are related to use of the decibel, owing to the impedance of the system. Because not all systems have the same impedance, different values will be obtained under this situation.

- dBm = 10 log (P1/0.001 watts)
- 1 volt in a 50 ohm system is equal to

$$dBm = 10 \log\left(\frac{1 \text{ volt}^2/50 \text{ ohms}}{0.001 \text{ watts}}\right) = 10 \log (20) = 13 \text{ dBm}$$

➪ Get MathML

- 1 volt in a 600-ohm system is equal to

$$dBm = 10 \log\left(\frac{1 \text{ volt}^2/600 \text{ ohms}}{0.001 \text{ watts}}\right) = 10 \log (1.67) = 2 \text{ dBm}$$

➪ Get MathML

Most engineers make a common mistake when performing decibel (logarithmic) math. This is known as the 6 dB problem. We must ask ourselves, "When does 6 dB not equal 6 dB?" Examples of this mistake follow. If the reference level is doubled, the logarithmic function increases by 6 dB. A three times increase in the reference is a 9.5 dB increase.

- 1000 µVolts = 60 dBµV
- 1000 µVolts = 60 dBµV

2000 µVolts = 66 dBµV

- 1000 µVolts = 60 dBµV

3000 µVolts = 69.5 dBµV

Appendix D - Conversion Tables

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Appendix D: Conversion Tables

Common Suffixes

Open table as spreadsheet

Suffix	Refers to
dBm	1 milliwatt
dBW	1 watt
dBμW	1 microwatt
dBV	1 volt
dBmV	1 millivolt
dBμV	1 microvolt
dBV/m	1 volt per meter
dBμV/m	1 microvolt per meter
dBA	1 amp
dBμA	1 microamp
dBμA/m	1 microamp per meter

Power and Voltage/Current Ratios

Open table as spreadsheet

Ratio	V or I in dB	P in dB
10^6	120	60
10^5	100	50
10^4	80	40
10^3	60	30
10^2	40	20
10	20	10
9	19.08	9.54
8	18.06	9.03
7	16.9	8.45
6	15.56	7.78
5	13.98	6.99
4	12.04	6.02
3	9.54	4.77
2	6.020	3.01
1	0	0
	-20	-10

10^{-1}		
10^{-2}	-40	-20
10^{-3}	-60	-30

dB	Power Ratio	Voltage/Current Ratio
120	10^{12}	10^{6}
100	10^{10}	10^{5}
80	10^{8}	10^{4}
60	10^{6}	10^{3}
40	10^{4}	10^{2}
30	10^{3}	32
20	10^{2}	10
10	10.0	3.2
6	4.0	2.0
3	2.0	1.4
0	1.0	1.0
-3	0.50	0.71
-6	0.25	0.50
-10	0.10	0.32
-20	10^{-2}	0.10
-30	10^{-3}	0.03
-40	10^{-4}	10^{-2}
-60	10^{-6}	10^{-3}
-80	10^{-8}	10^{-4}
-100	10^{-10}	10^{-5}
-120	10^{-12}	10^{-6}

Conversion of dBV, dBmV, and dBµV

➡ Open table as spreadsheet

dBV	dBmV	dBµV
-120	-60	0
-100	-40	20
-80	-20	40
-60	0	60
-40	20	80
-20	40	100
0	60	120
20	80	140
40	100	160
60	120	180

Conversion of Volt/m to mW/cm^2 for Linear and dB

Scales

➡ Open table as spreadsheet

V/m	dBµV/m	mW/cm^2	$dBmW/cm^2$
1.00×10^{-6}	0	2.67×10^{-16}	-155.8
1.00×10^{-5}	20	2.67×10^{-14}	-135.8
1.00×10^{-4}	40	2.67×10^{-12}	-115.8
1.00×10^{-3}	60	2.67×10^{-10}	-95.8
1.00×10^{-2}	80	2.67×10^{-8}	-75.8
1.00×10^{-1}	100	2.67×10^{-6}	-55.8
1.00	120	2.67×10^{-4}	-35.8
$1.00 \times 10^{+1}$	140	2.67×10^{-2}	-15.8
$1.00 \times 10^{+2}$	160	2.67	-4.2
$1.00 \times 10^{+3}$	180	267	-24.2
$1.00 \times 10^{+6}$	6	1.06×10^{-15}	-149.7
$2.00 \times 10^{+6}$	12	4.24×10^{-15}	-143.7
$6.00 \times 10^{+6}$	15	9.55×10^{-15}	-140.2
$8.00 \times 10^{+6}$	18	1.70×10^{-14}	-137.7

dBµV versus dBm for Z = 50Ω

➡ Open table as spreadsheet

dBµV	µV	dBm	Power Level
-20	0.1	-127	0.0002 pW
-10	0.316	-117	0.002 pW
0	1.0	-107	0.02 pW
5	1.778	-102	0.063 pW
7	2.239	-100	0.1 pW
10	3.162	-97	0.2 pW
15	5.623	-92	0.632 pW
20	10.0	-87	2.0 pW
30	0.03162	-77	0.02 pW
40	0.10	-67	0.2 pW
50	0.312	-57	2.0 pW
60	1.0	-47	20.0 pW
70	3.162	-37	0.2 µW
80	10.0	-27	2.0 µW
90	31.62	-17	20.0 µW
100	100.0	-7	2000.0 µW
120	1.0V	+13	20.0 mW

Frequency—Wavelength—Skin Depth

➡ Open table as spreadsheet

Frequency	λ	λ/2π	Skin Depth
10 Hz	30,000 km	4,800 km	820 mil

60 Hz	5,000 km	800 km	340 mil
100 Hz	3,000 km	480 km	260 mil
400 Hz	750 km	120 km	130 mil
1 kHz	300 km	48 km	82 mil
10 kHz	30 km	4.8 km	26 mil
100 kHz	3 km	480 m	8.2 mil
1 MHz	300 m	48 m	2.6 mil
10 MHz	30 m	4.8 m	0.8 mil
100 MHz	3 m	0.48 m	0.3 mil
1 GHz	30 cm	4.8 cm	0.08 mil
10 GHz	3 cm	4.8 mm	0.03 mil
λ = wavelength			
λ/2π = near field to far field distance conversion			
distance: metric (meters)			

Frequency—Wavelength Conversion

➡ Open table as spreadsheet

To determine the frequency of a signal and its related wavelength, use the following conversion equations.	
f(MHz) = 300/λ(MHz)	f(MHz) = 984/λ (ft)
λ (m) = 300/f(MHz)	λ (ft) = 984/f(MHz)
λ = wavelength, f = frequency	

Throughout this book, reference is made to critical frequencies or high-threat clock and periodic signal traces that have a length greater than λ/20. A summary of miscellaneous frequencies and their respective wavelength distance is shown in the following table, based on the equations shown above.

Frequency of Interest	λ/20 Wavelength Distance
10 MHz	1.5 m (5 ft)
27 MHz	0.56 m (1.8 ft)
35 MHz	0.43 m (1.4 ft)
50 MHz	0.33 m (12 in)
80 MHz	0.19 m (7.4 in)
100 MHz	0.15 m (5.9 in)
160 MHz	9.4 cm. (3.7 in)
200 MHz	7.5 cm (3 in)
400 MHz	3.75 cm (1.5 in)
600 MHz	2.5 cm (1.0 in)
1000 MHz	1.5 cm (0.60 in)

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by Mark I. Montrose

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